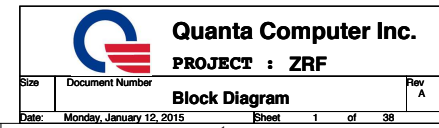


01

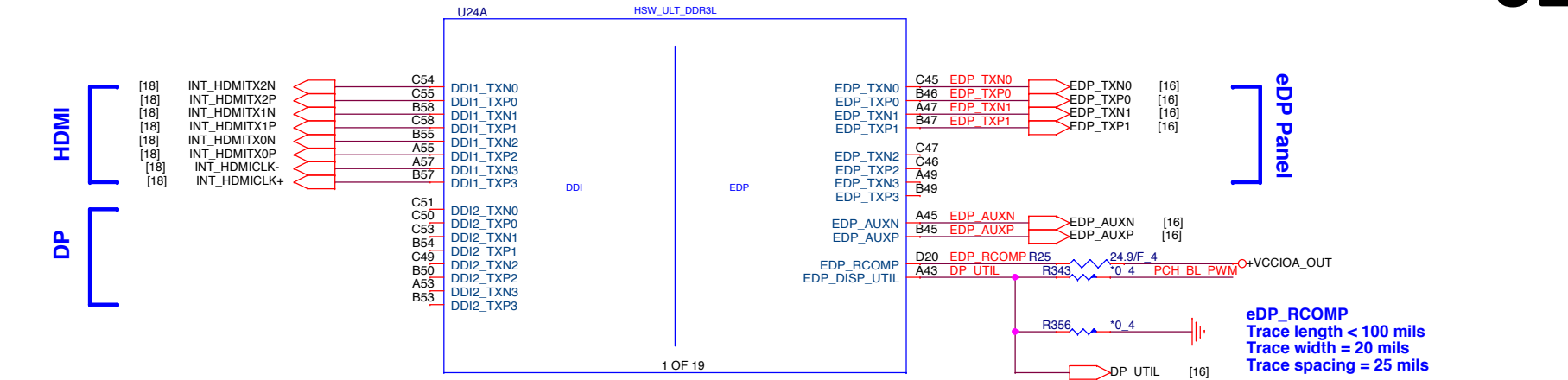


Haswell ULT (DISPLAY,eDP)

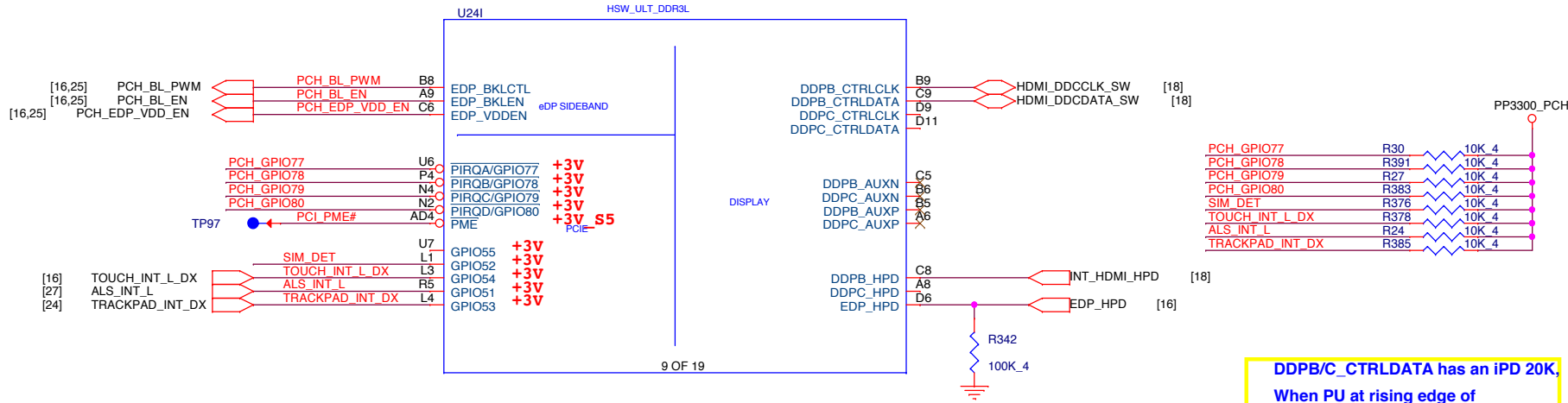
02

HDMI
DP

eDP Panel



eDP_RCOMP
Trace length < 100 mils
Trace width = 20 mils
Trace spacing = 25 mils



Haswell C-1 2c BGA 1.6GHz ULV 15W 2+2 i5-4200U QS for proto/AJ0QEVEVT01

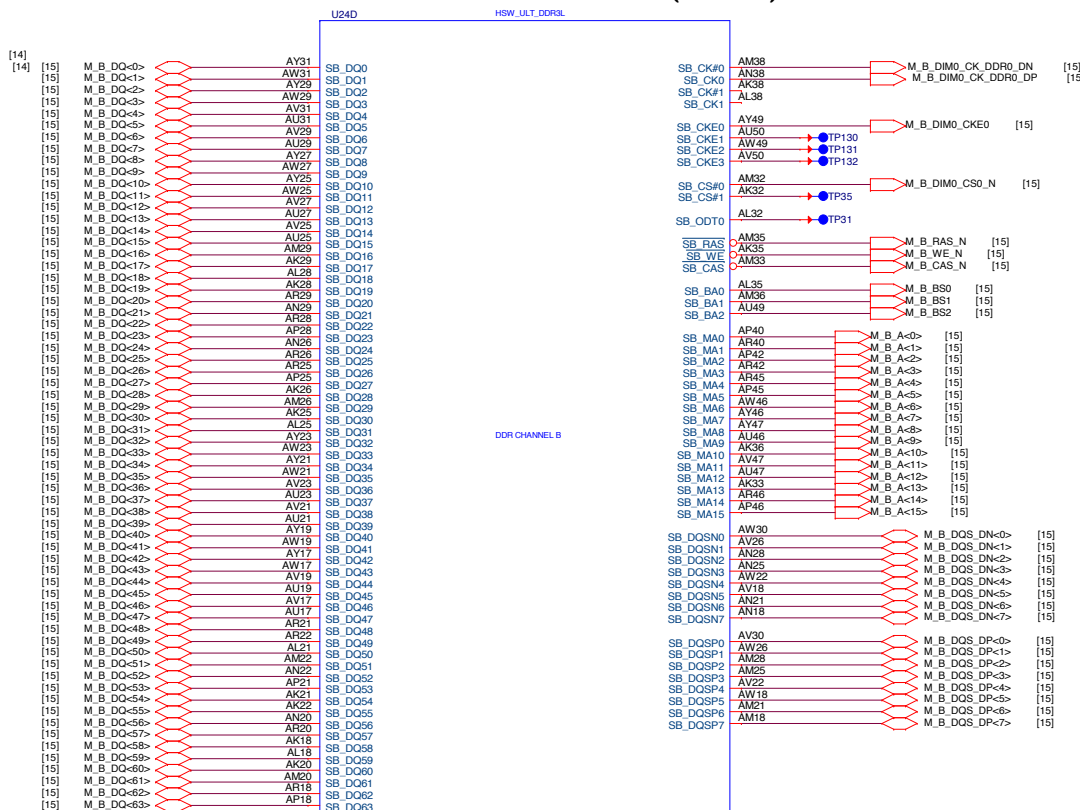
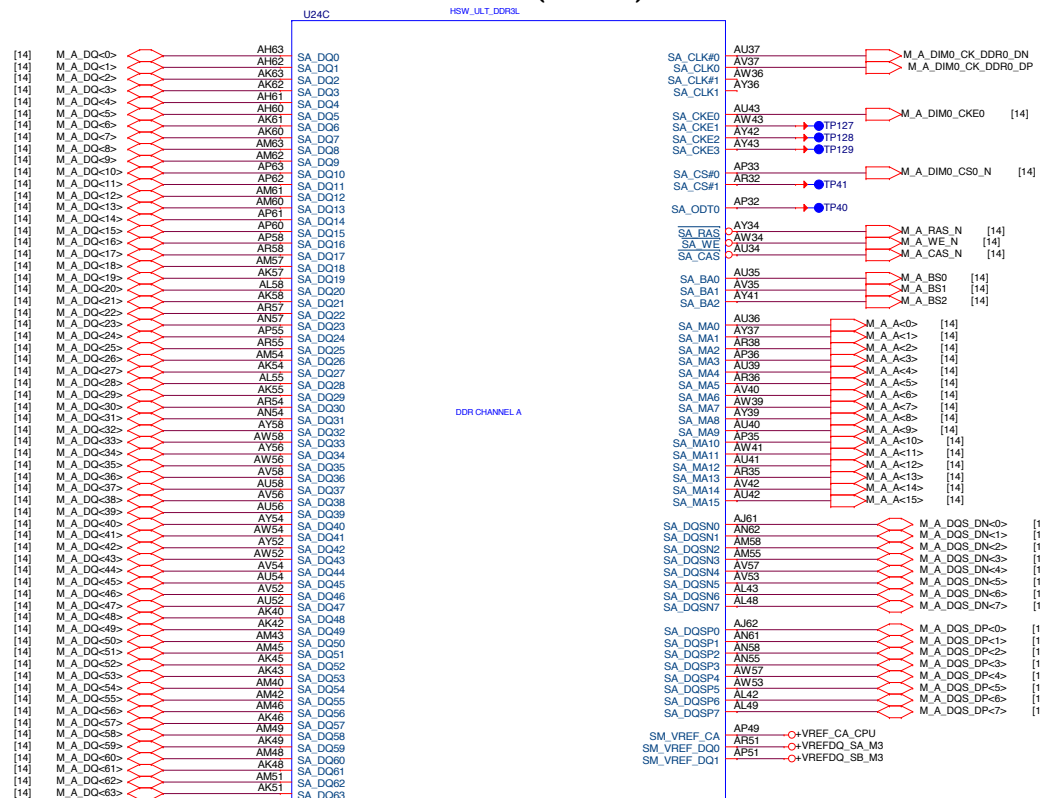
DDPB/C_CTRLDATA has an iPD 20K.
When PU at rising edge of
PCH_PWROK, the DDI port will
be detected



Quanta Computer Inc.

PROJECT : ZRF

Size	Document Number	Rev A
	Haswell 1/5 (DDI/eDP)	
Date:	Monday, January 12, 2015	Sheet 2 of 38

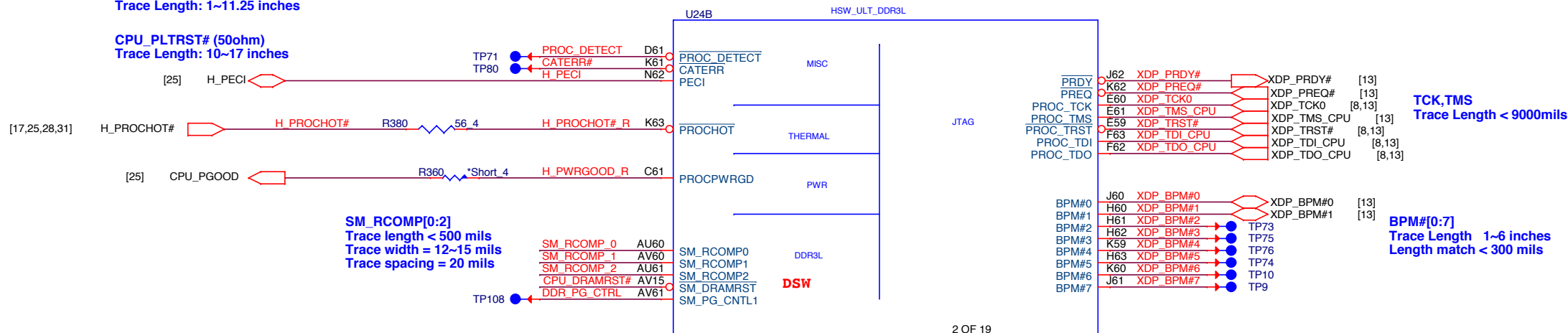
Haswell ULT (DDR3L)**Haswell Processor (DDR3L)**

Haswell ULT (SIDEBAND)

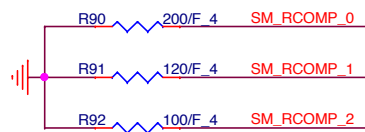
H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 inches

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

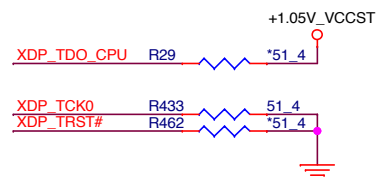
CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches



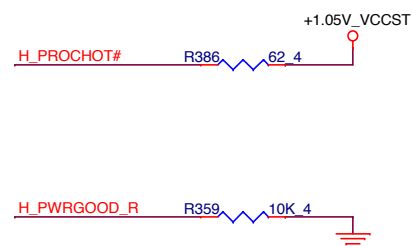
DRAM COMP



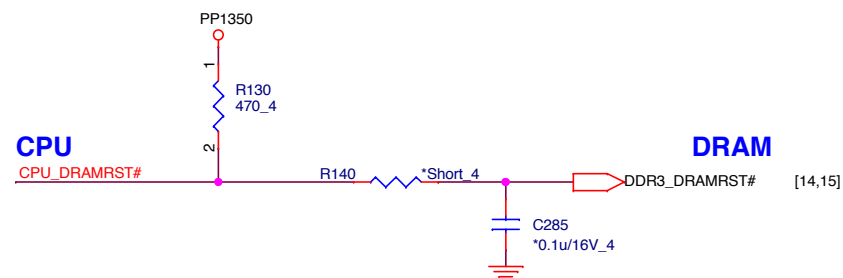
XDP PU/PD



PU/PD of CPU



DRAMRST

**Quanta Computer Inc.**

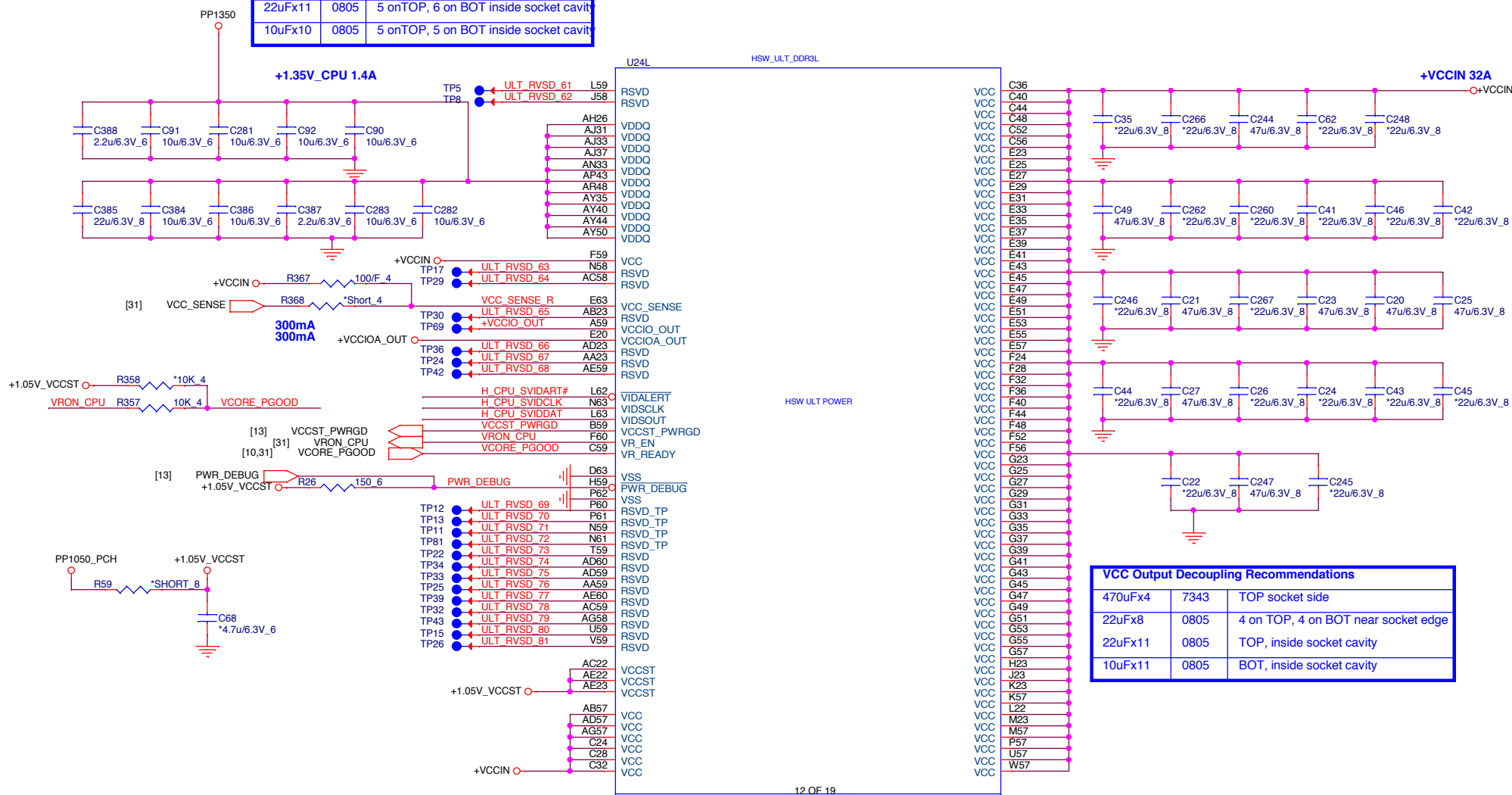
PROJECT : ZRF

Size	Document Number	Rev
	Haswell 3/5 (SideBand)	A
Date:	Monday, January 12, 2015	Sheet 4 of 38

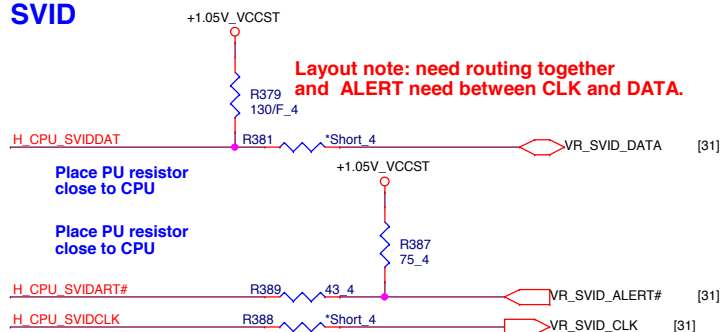
Date: Monday, January 12, 2015 Sheet 4 of 38

Haswell ULT (POWER)

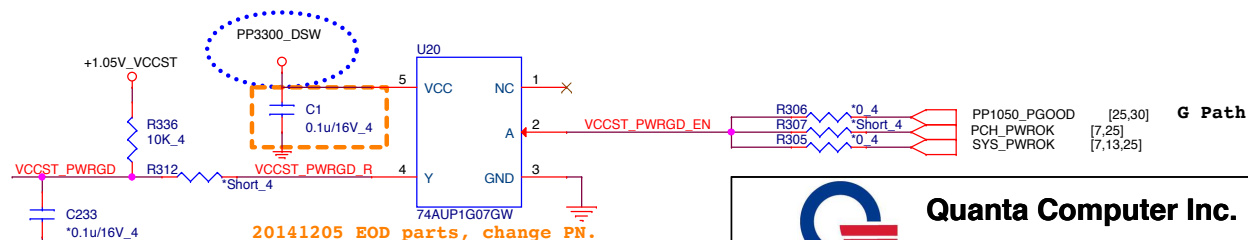
VDDQ Output Decoupling Recommendations		
330uFx2	7343	BOT socket side
22uFx11	0805	5 on TOP, 6 on BOT inside socket cavity
10uFx10	0805	5 on TOP, 5 on BOT inside socket cavity



SVID



VCCST PWRGD

**Quanta Computer Inc.**

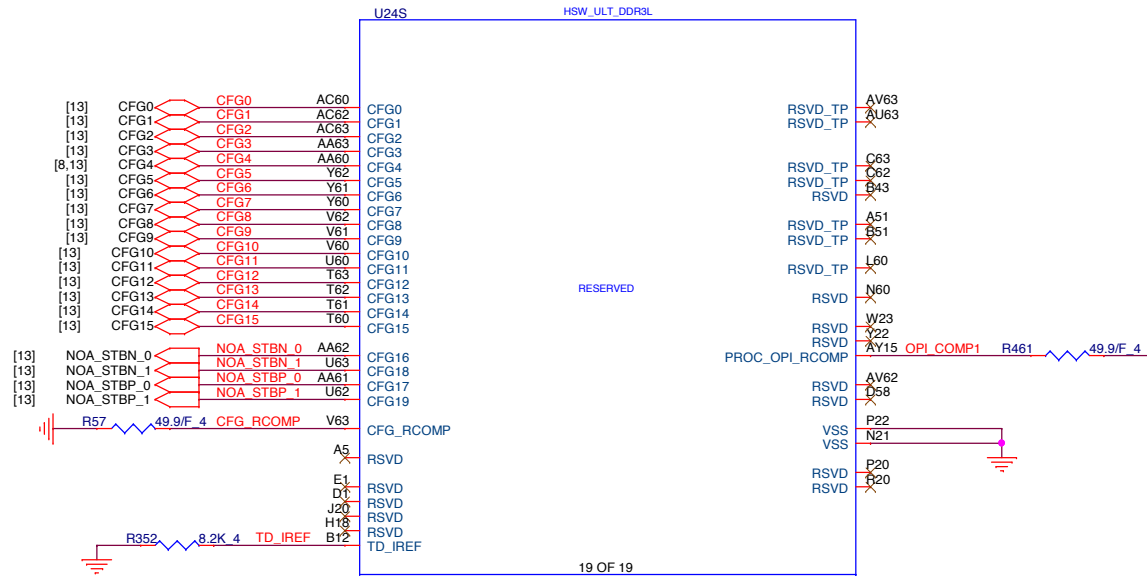
PROJECT : ZRF

Haswell 4/5 (POWER)

Date: Monday, January 12, 2015 Sheet 5 of 38

Haswell ULT (CFG,RSVD)

06



19 OF 19

Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	CFG0 R417 *1K 4
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	CFG1 R423 *1K 4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R409 *1K 4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R403 *1K 4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R394 *1K 4
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R56 *1K 4

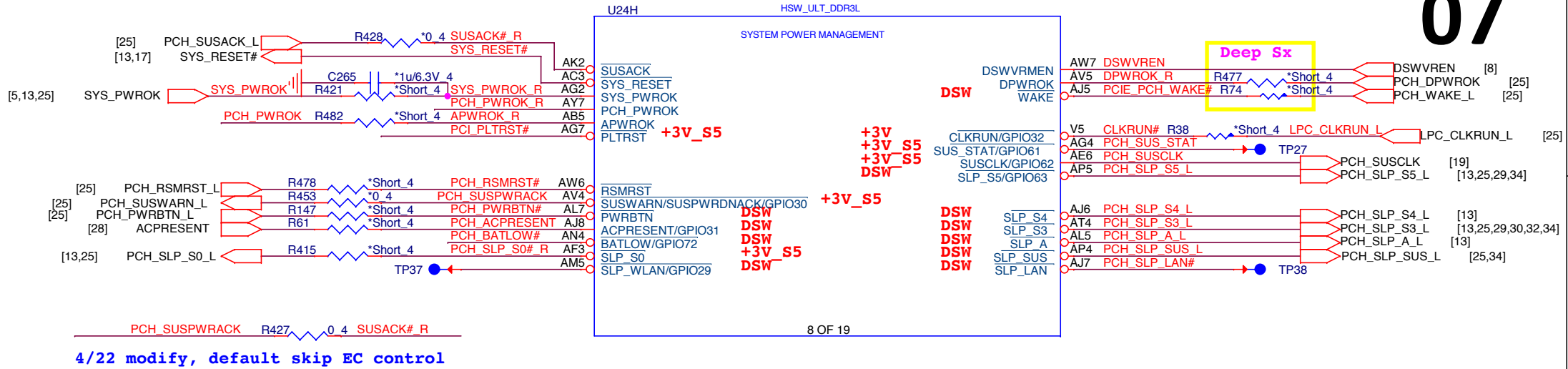


Quanta Computer Inc.
PROJECT : ZRF

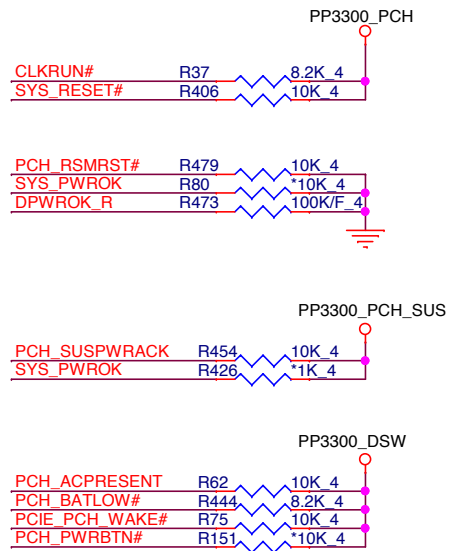
Size	Document Number	Rev
	Haswell 5/5 (CFG/GND)	A
Date:	Monday, January 12, 2015	Sheet 6 of 38

Haswell ULT PCH (PM)

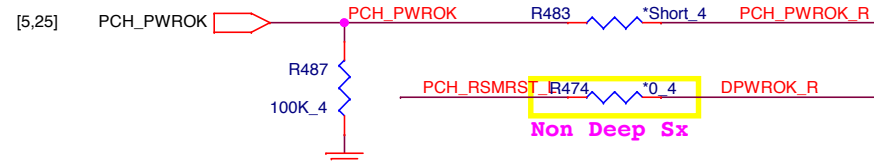
07



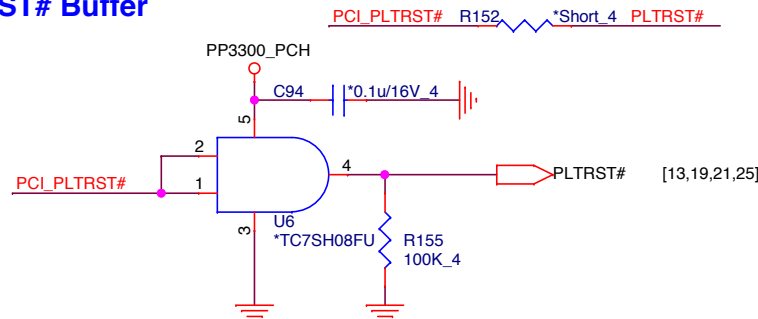
PCH PM PU/PD



PCH PWROK



PLTRST# Buffer



4/22 modify, default is bypass PLTRST#

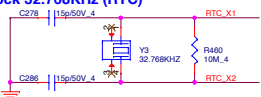


Quanta Computer Inc.

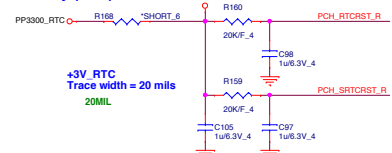
PROJECT : ZRF

Size	Document Number	Rev
	PCH 1/6 (PM)	A
Date:	Monday, January 12, 2015	Sheet 7 of 38

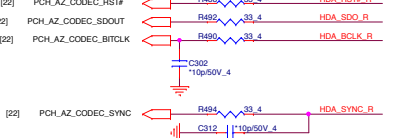
RTC Clock 32.768KHz (RTC)



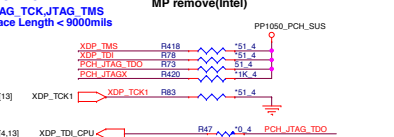
RTC Circuitry (RTC)

+3V_RTC
Trace width = 30 mils+3V_RTC
Trace width = 20 mils

HDA



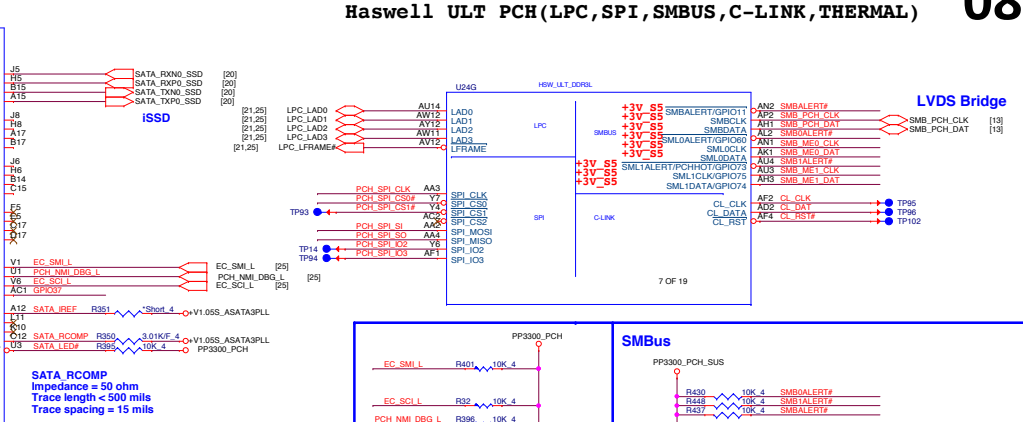
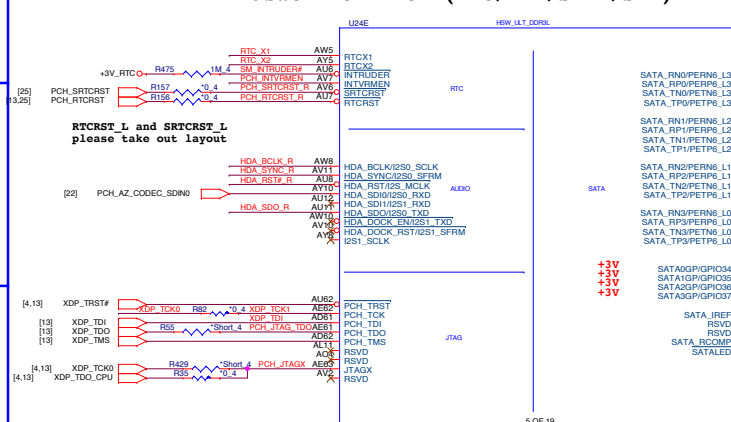
PCH JTAG



ULT Strapping Table

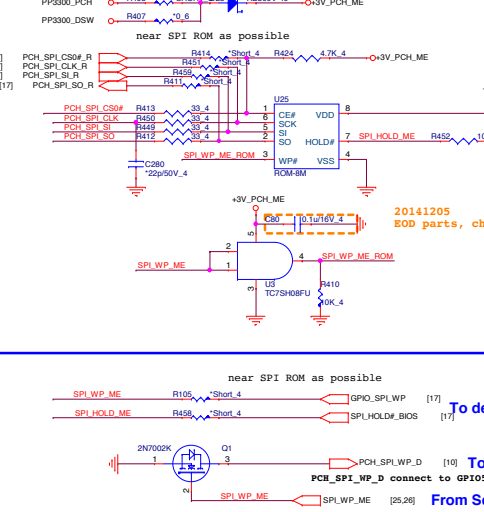
Pin Name	Strap description	Sampled	Configuration	Note
GPIO81 (SPKR)	No reboot on TCO Timer expiration	PWR0K	0 = Default enable (IPD 20K) 1 = Disable No-Reboot mode	PP3300_PCH R400 *1K 4 SPKR [10,22]
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWR0K	0 = Default can program ME (IPD 20K) 1 = can't program ME	HDA_SDO_R R493 *0.4 PCH HDA_SDO [85]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	1 = Should be always pull-up	+3V_RTC R484 *330K 4 PCH INTRVDMEN R489 *330K 4
GPIO66	Top-Block Swap override		0 = Default disable (IPD 30K) 1 = Enable TBS function	PP3300_PCH R330 *1K 4 GPIO66 R340 *1K 4
GPIO86	Boot BIOS Strap Bit		0 = Default SPI (IPD 20K) 1 = LPC	PP3300_PCH R1 *1K 4 GPIO86 R7 *1K 4
GPIO15	TLS (Transport layer security)		0 = Default enable w/o confidentiality (IPD 20K) 1 = Default enable with confidentiality	PP3300_PCH_SUS R50 *0.2K 4 GPIO15 R58 *1K 4
CFG4	DP presence strap		0 = Enable an external display port is connected to the eDP 1 = disable	[6,13] CFG4 R64 *1K 4
DSWVREN	Deep Sx well on the VR enable		1 = Should be always pull-up	[7] DSWVREN R476 *330K 4 DSWVREN R472 *330K 4

Haswell ULT PCH (RTC/HDA/SATA/SPI)

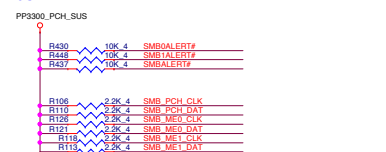


PCH dual I/O SPI ROM

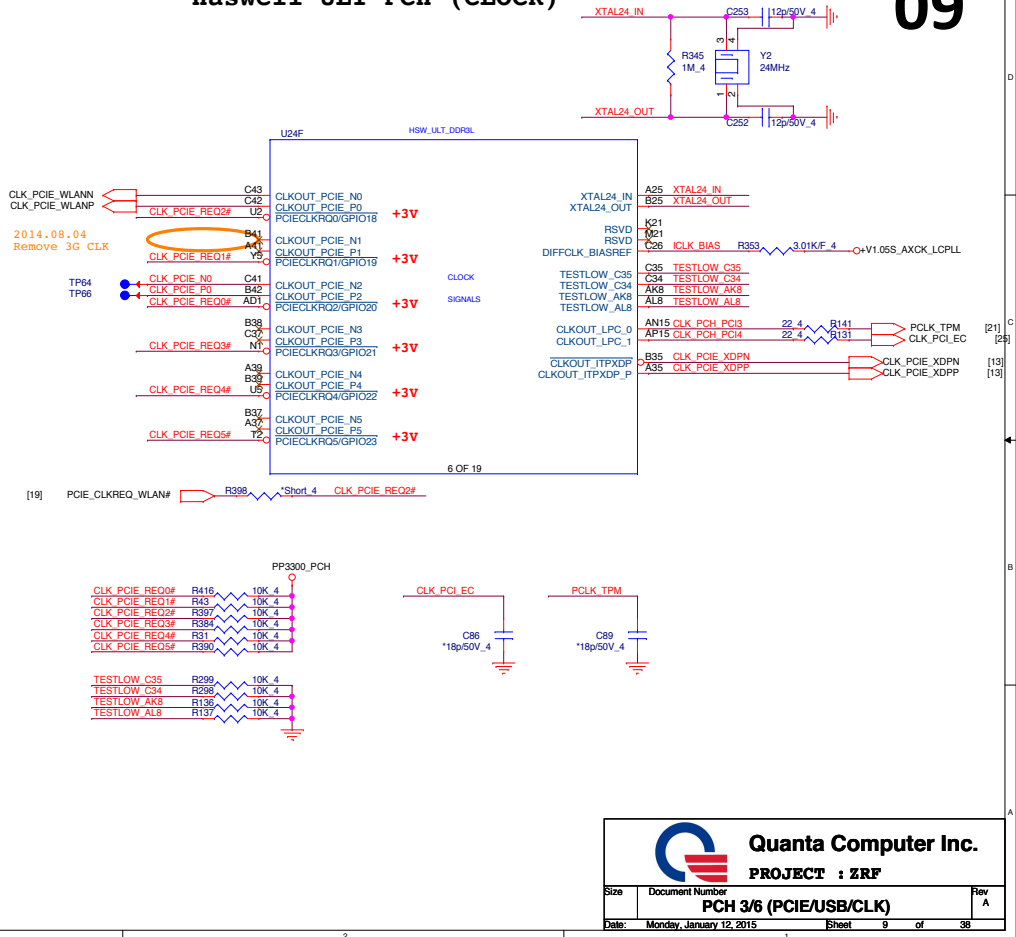
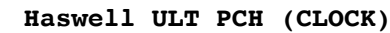
W25Q64FVSSIG(SOIC) / AKE3EFPON06----->8MB

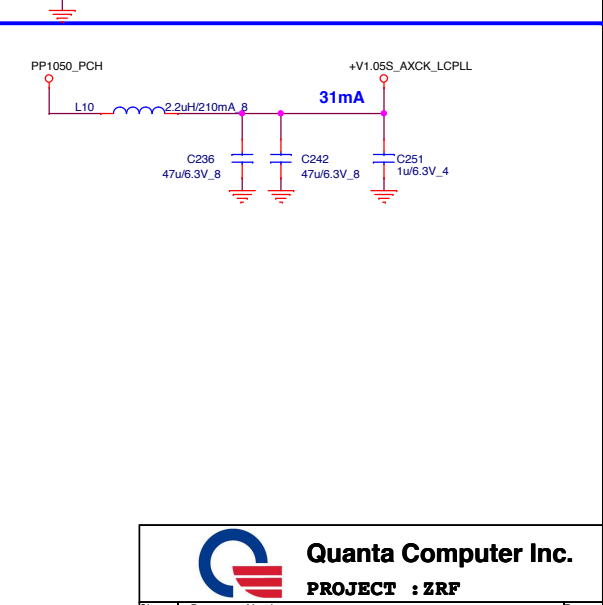
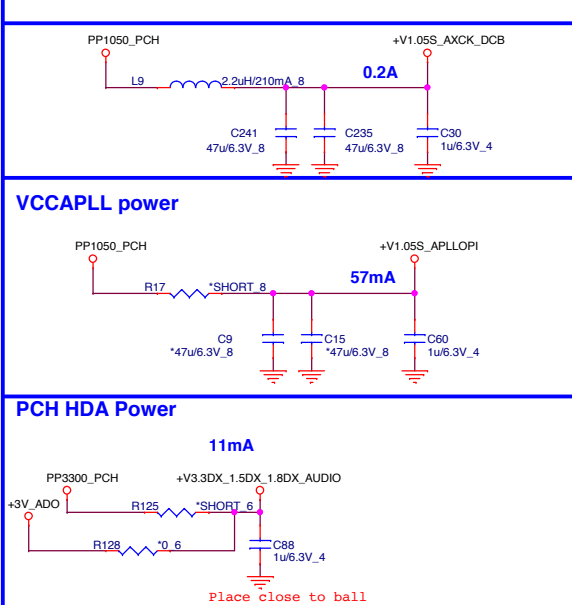


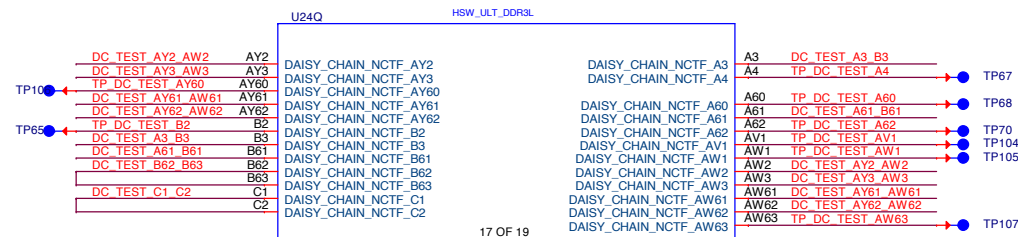
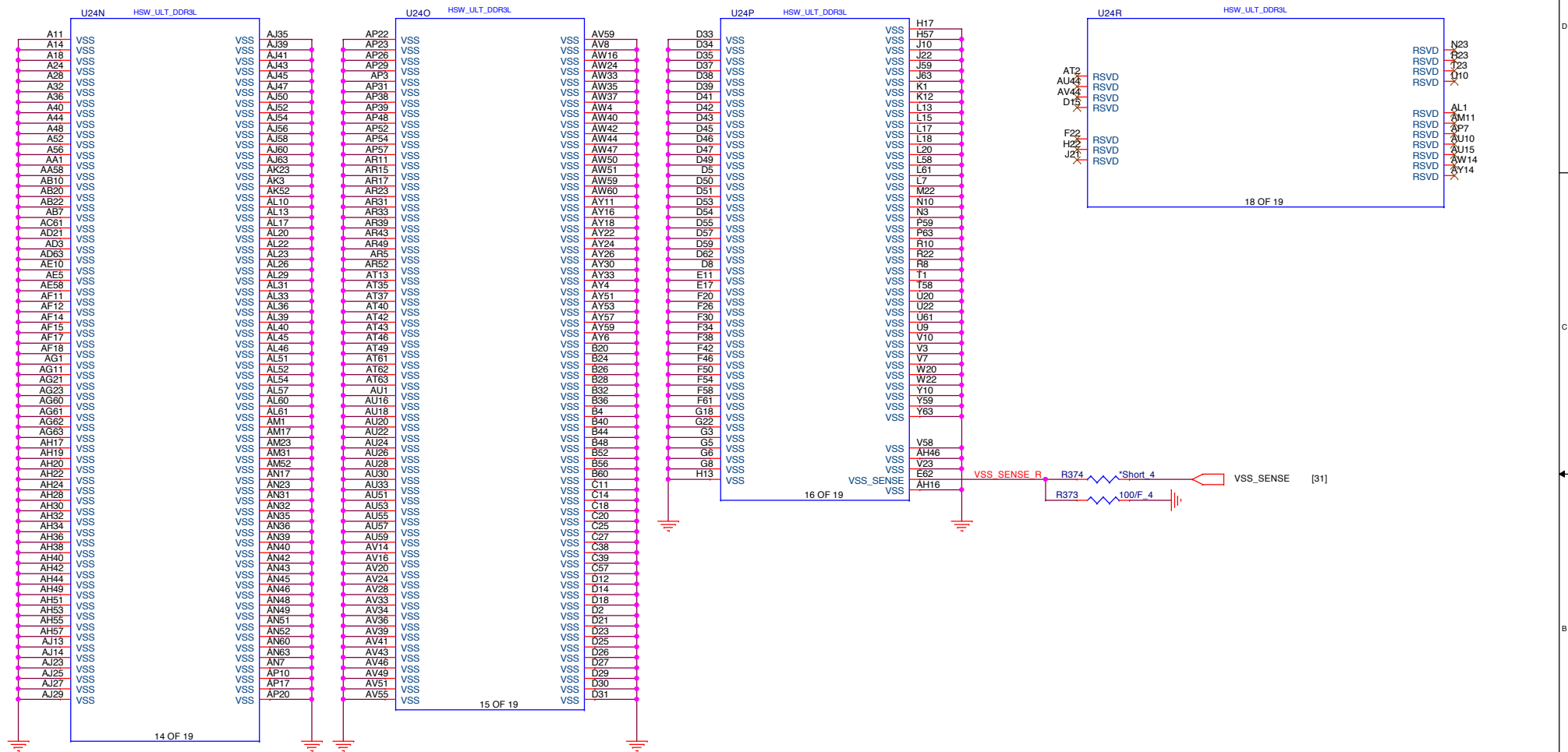
SMBus



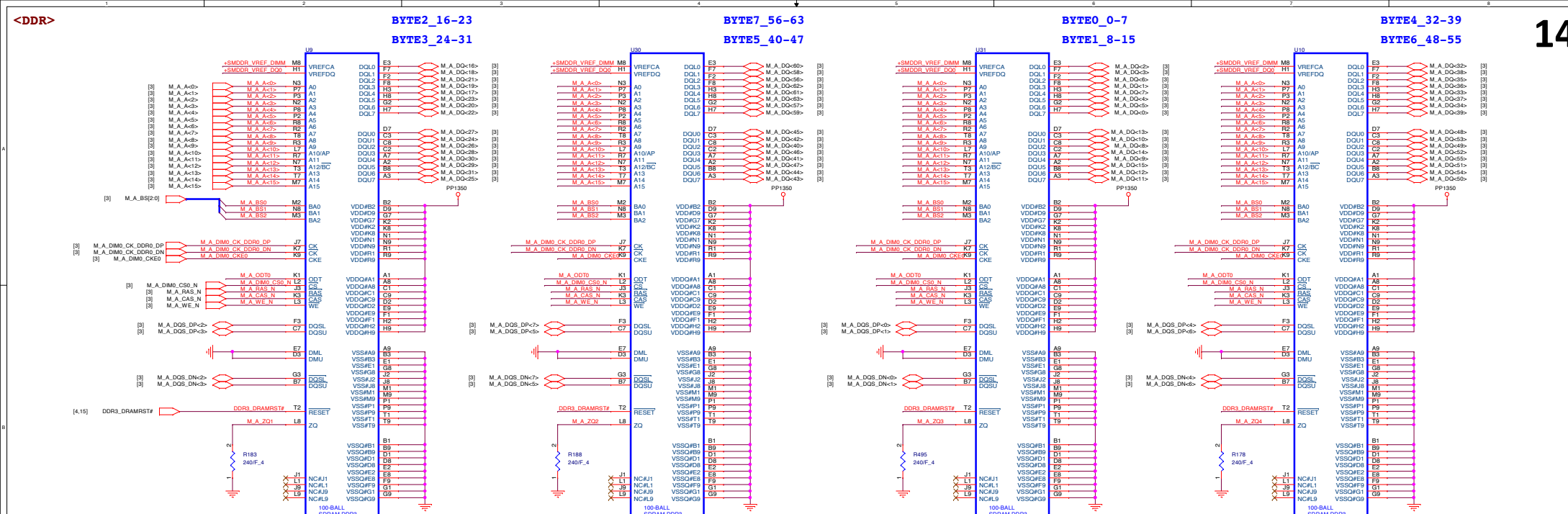
09



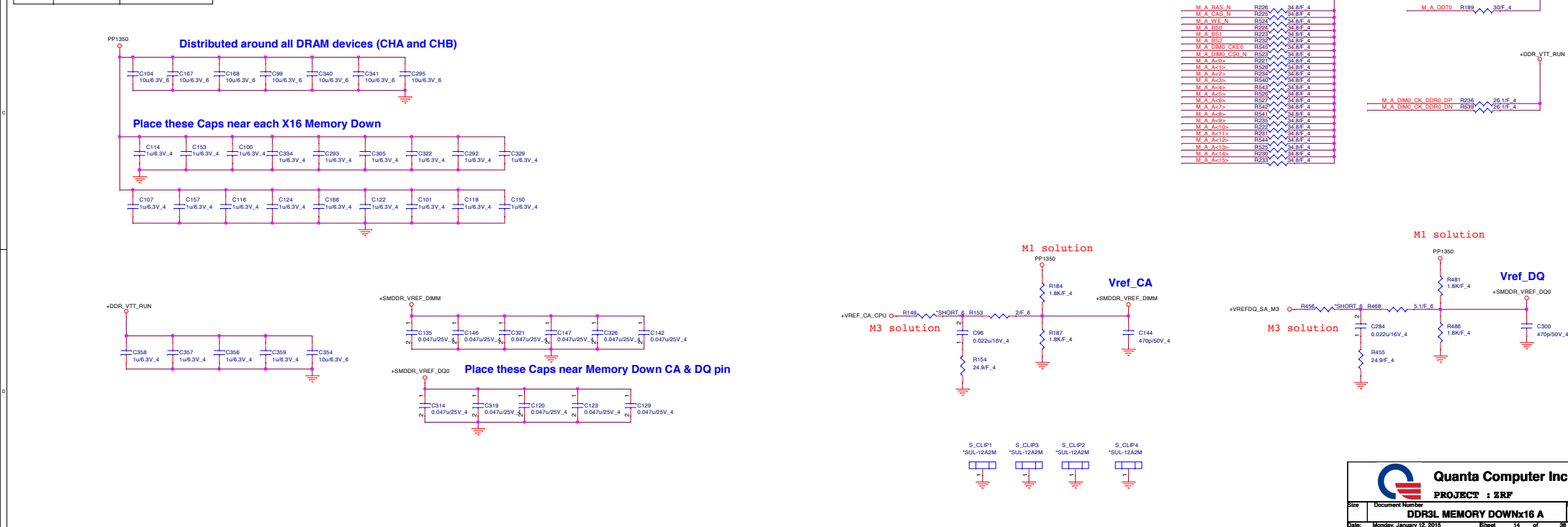


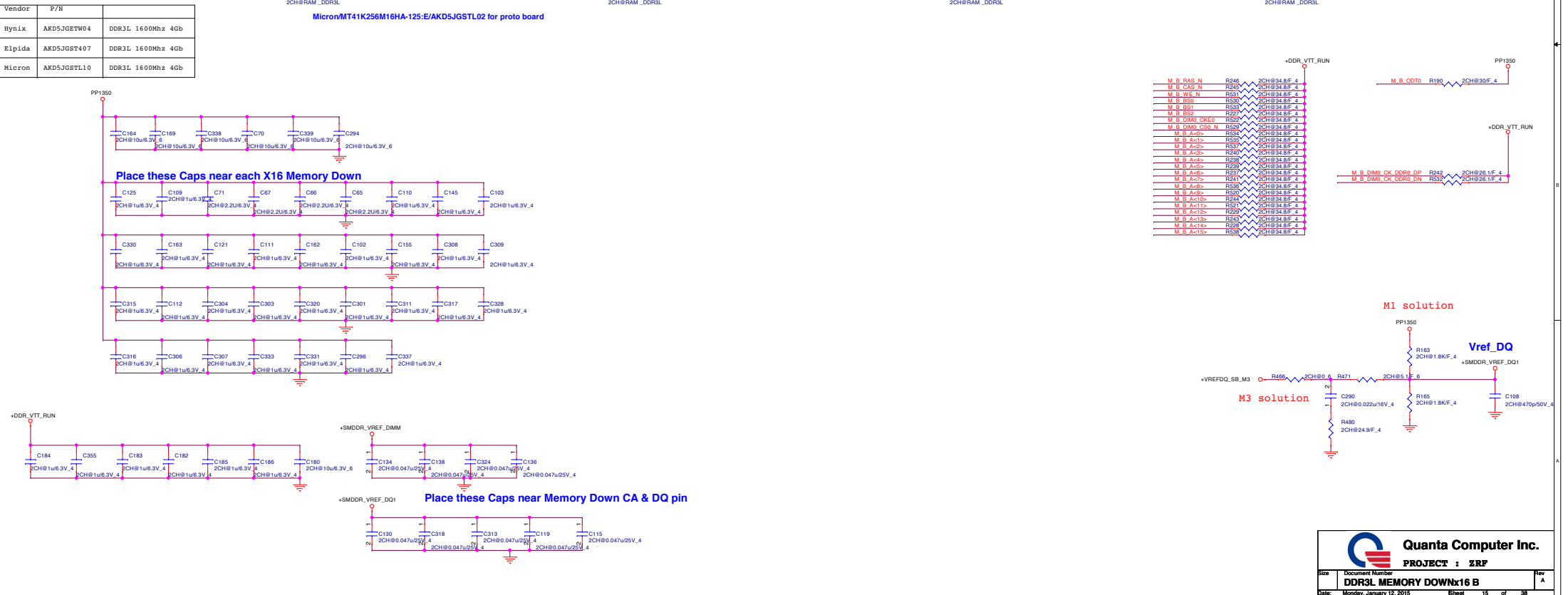
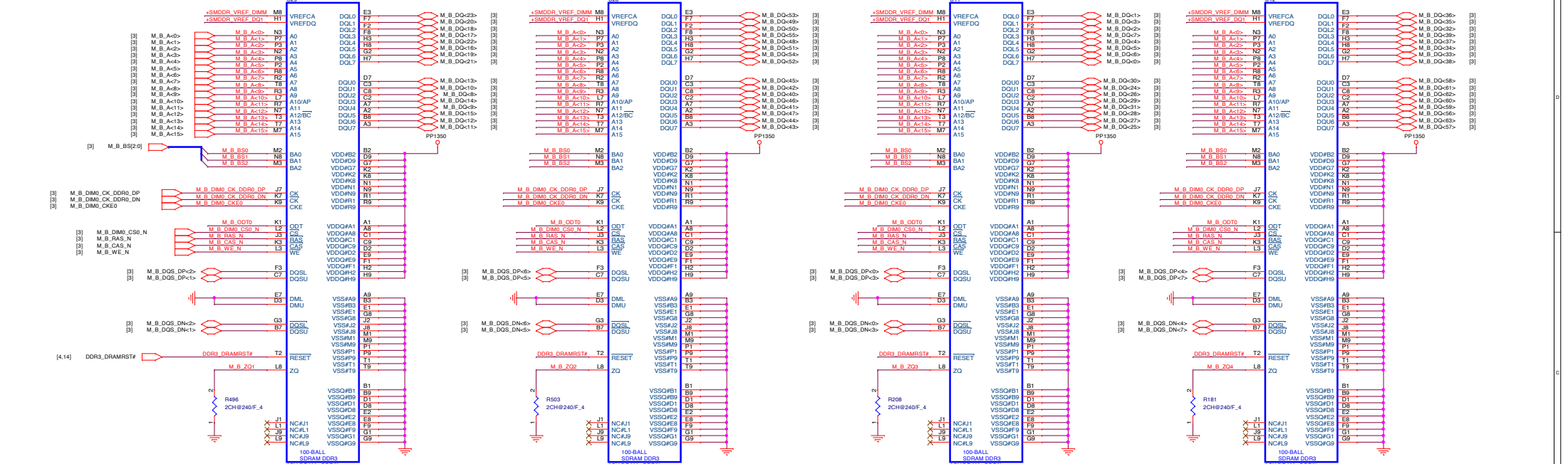
Haswell ULT (GND)



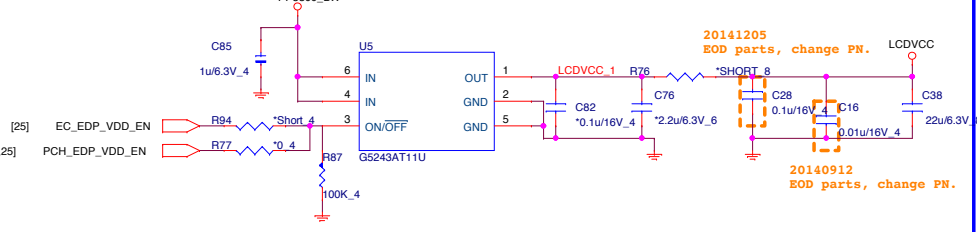


Vendor	P/N	
Hynix		
Elpida	AKD5JGST400	DDR3L 1333Mhz 4Gb
	AKD5JGST404	DDR3L 1600Mhz 4Gb

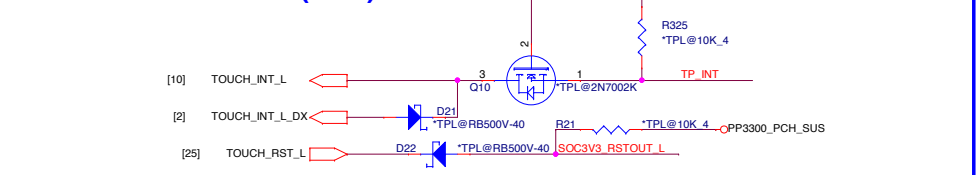




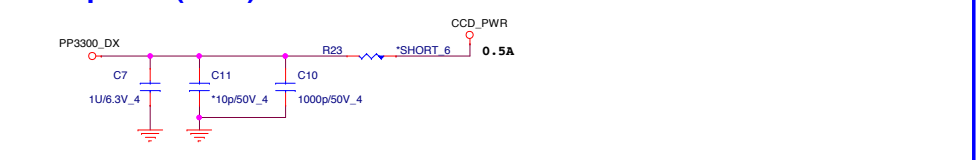
LVDS Power(LDS)



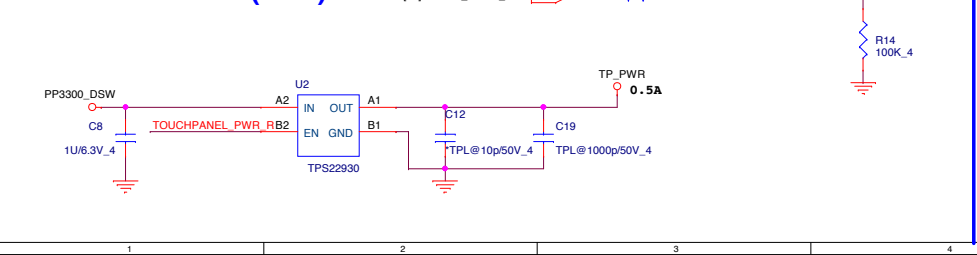
Touch Panel INT/RST(TSN)



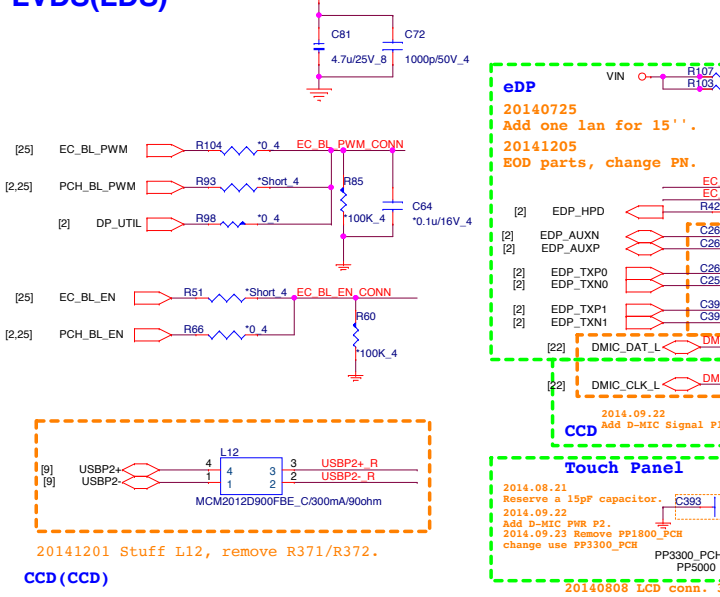
CCD power(CCD)



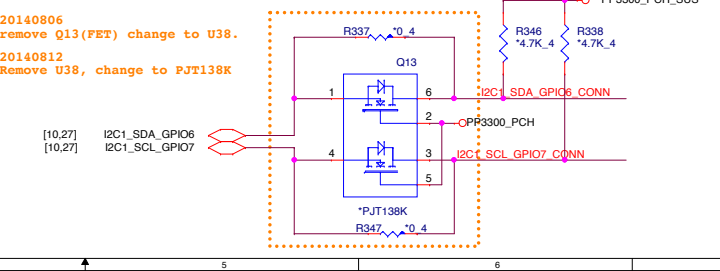
Touch Pad Power(TPD)



LVDS(LDS)



Touch Panel level shift(TSN)



LVDS CONN
DFHS40FS095
footprint lvds-cvs5402mlrb-nh-40p-1

16

eDP

20140725
Add one lan for 15''.

20141205
EOD parts, change PN.

CCD

2014.08.21
Reserve a 15pF capacitor.

2014.09.22
Add D-MIC PWR P2.

2014.09.23
Remove PP1800_PCH
change use PP3300_PCH

Touch Panel

20140808 LCD conn. 30pin change to 40pin,
1 LEN change to 2 LEN.

20140827 LCD conn. change PN / footprint
same as ZQ0.

20140930 Change LCD conn. footprint.

20141021 LCD conn. footprint return to ZQ0.

EDP_50406-04071-001

Quanta Computer Inc.

PROJECT : ZRF

LVDS/CCD/DMIC/TS

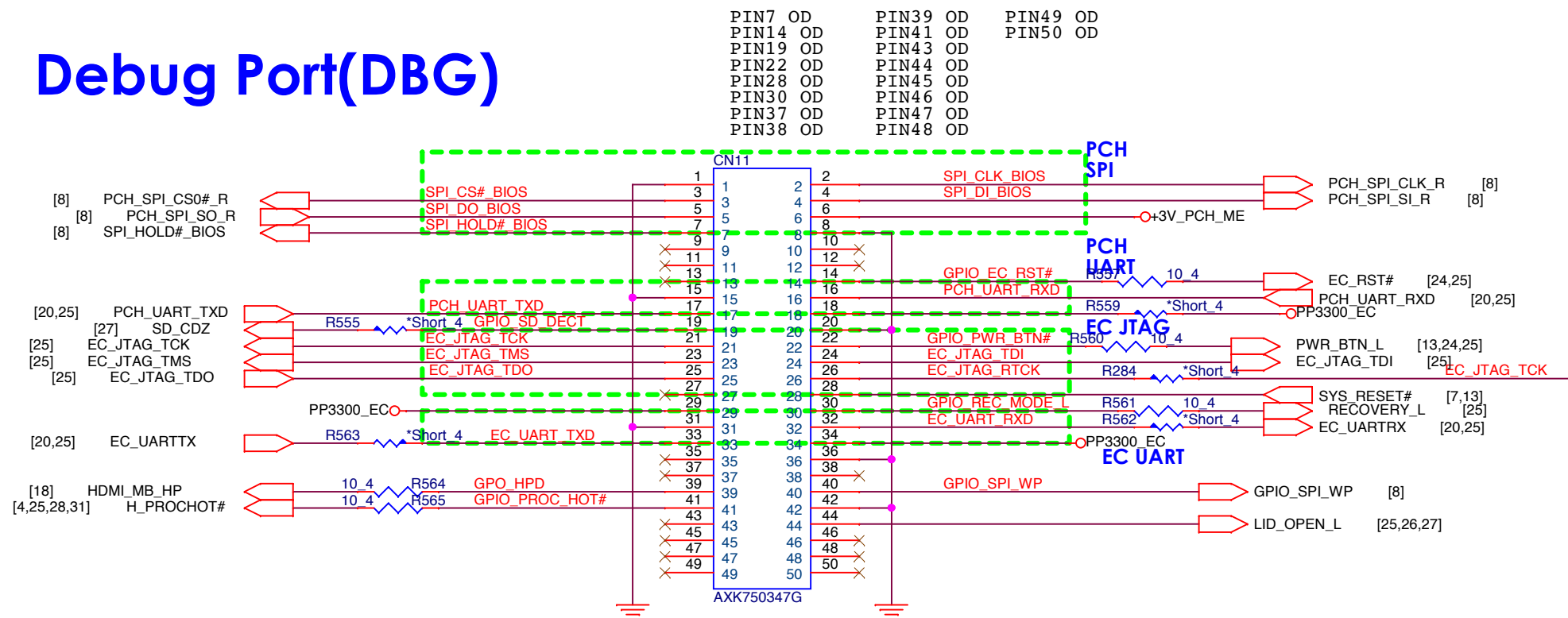
Size Document Number

Date: Monday, January 12, 2015

Sheet 16 of 38

Rev A

Debug Port(DBG)

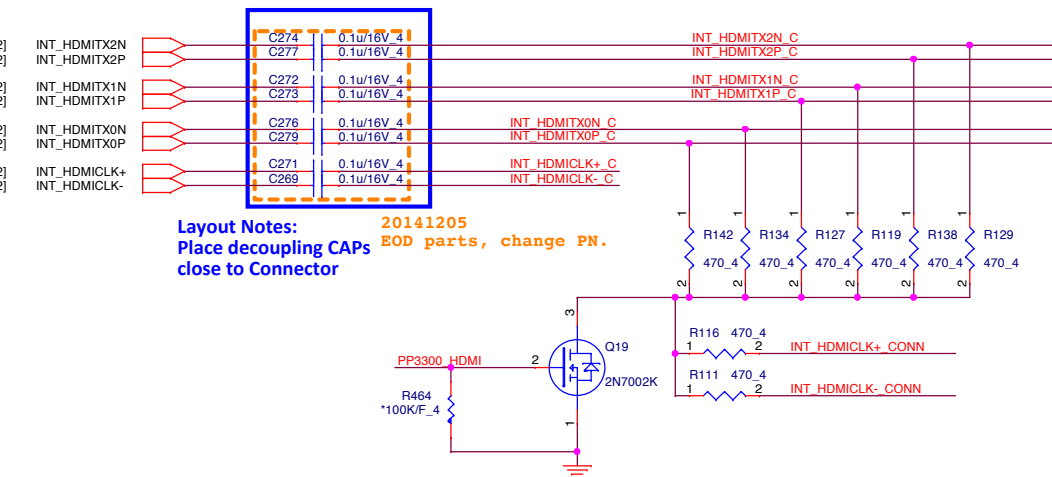


Quanta Computer Inc.

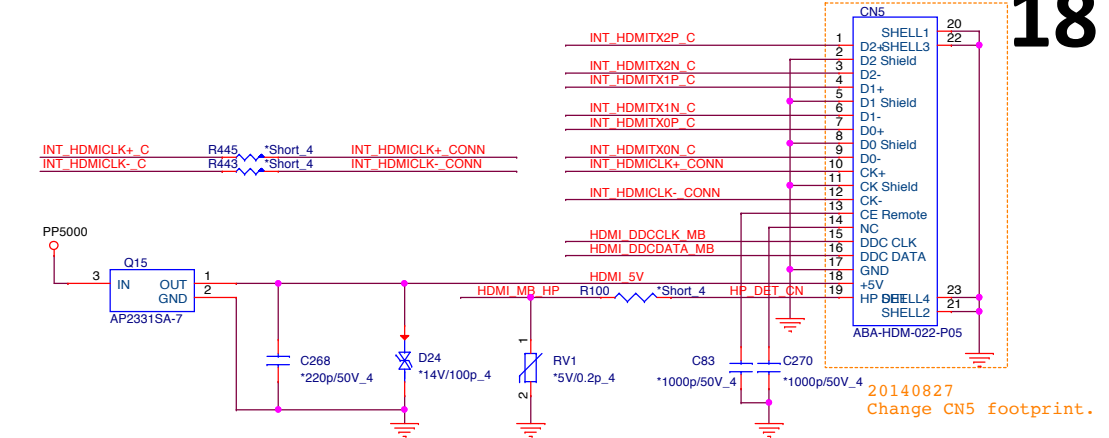
PROJECT : ZRF

Size	Document Number	Rev A
Google Debug		
Date:	Monday, January 12, 2015	Sheet 17 of 38

HDMI Cost Reduced level shift (HDM)

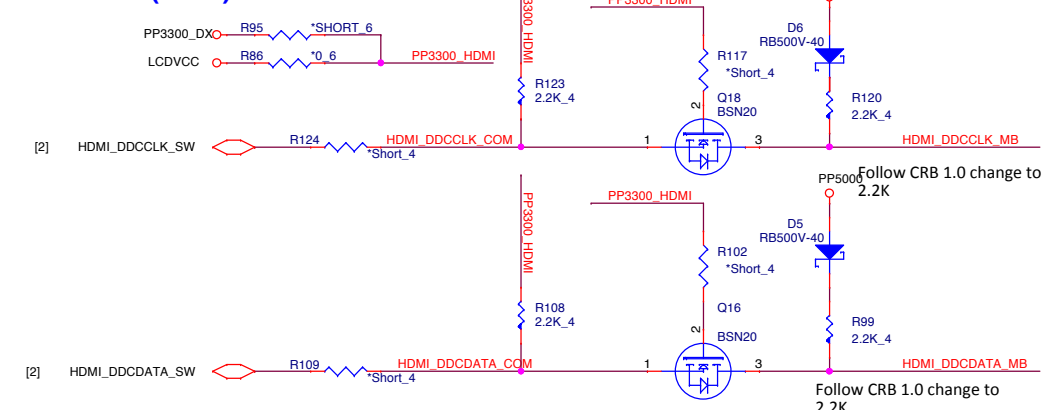


HDMI connector (HDM)

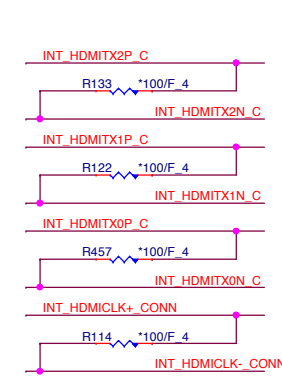


18

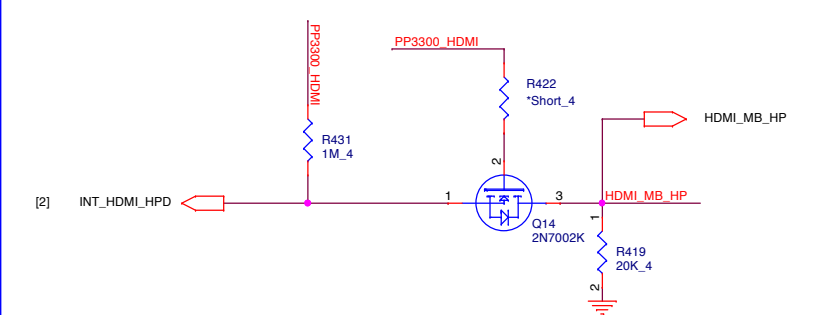
HDMI DDC (HDM)



EMI (HDM)



HDMI-detect (HDM)

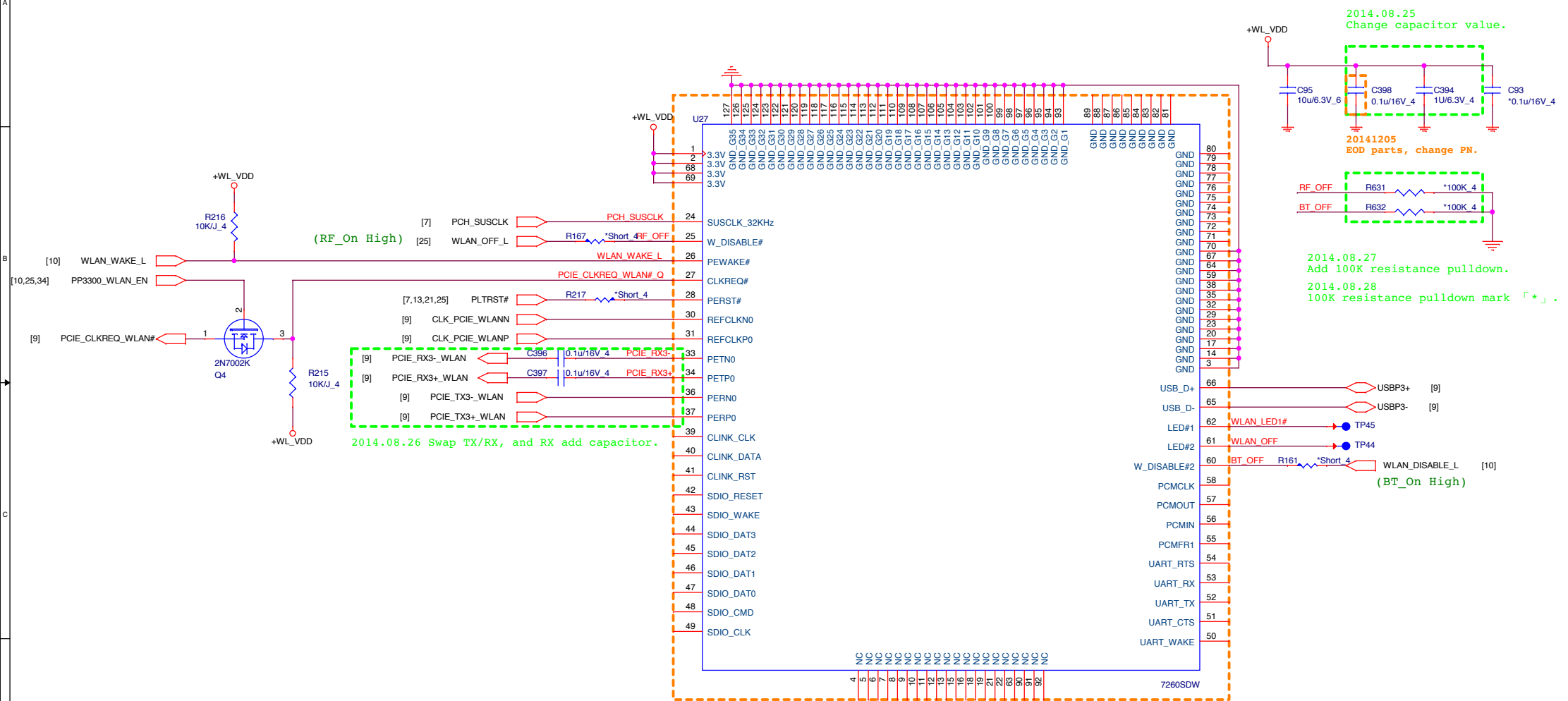


Quanta Computer Inc.


PROJECT : ZRF

HDMI

Size	Document Number	Rev	A
Date:	Monday, January 12, 2015	Sheet	18 of 38

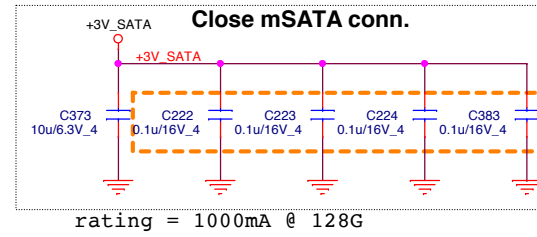


- 20140820 On board IC change to same as ZS8 connector
- 20140822 Return to another wifi onboard module 7260SDW
- 20140826 Change wifi onboard module 7260SDW footprint
- 20140909 Change wifi onboard module 7260SDW footprint
- 20141014 Change wifi onboard module 7260SDW PN.

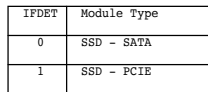


Quanta Computer Inc.
PROJECT : ZRF

Size	Document Number	Rev A
WIFI / BT		
Date: Monday, January 12, 2015	Sheet 19 of 38	

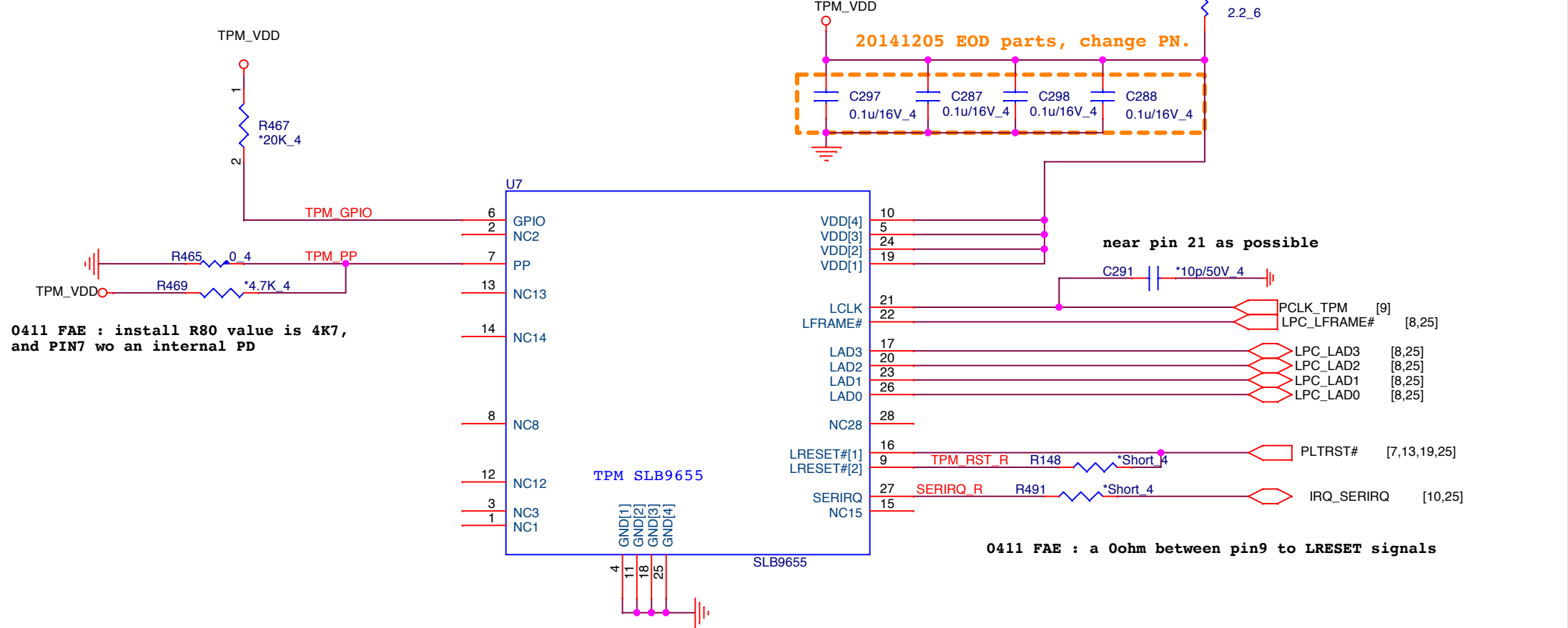



```
rating = 1000mA @ 128G
```



TPM (TPM)

21



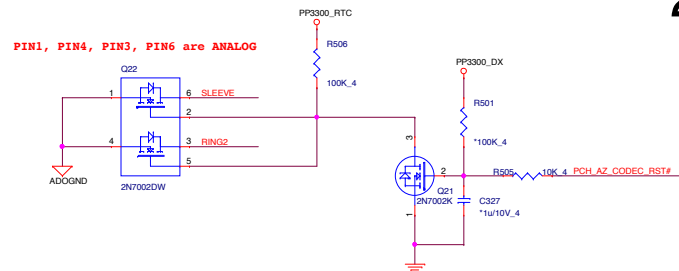


Quanta Computer Inc.

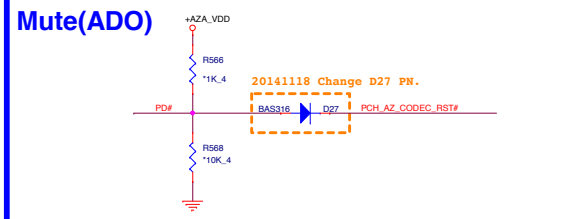
PROJECT : ZRF

Size	Document Number	Rev
	TPM SLB9655 / LED	A
Date:	Monday, January 12, 2015	Sheet 21 of 38

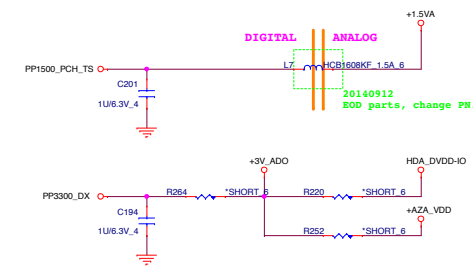
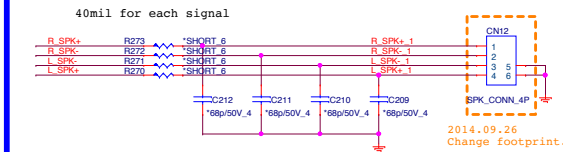
22



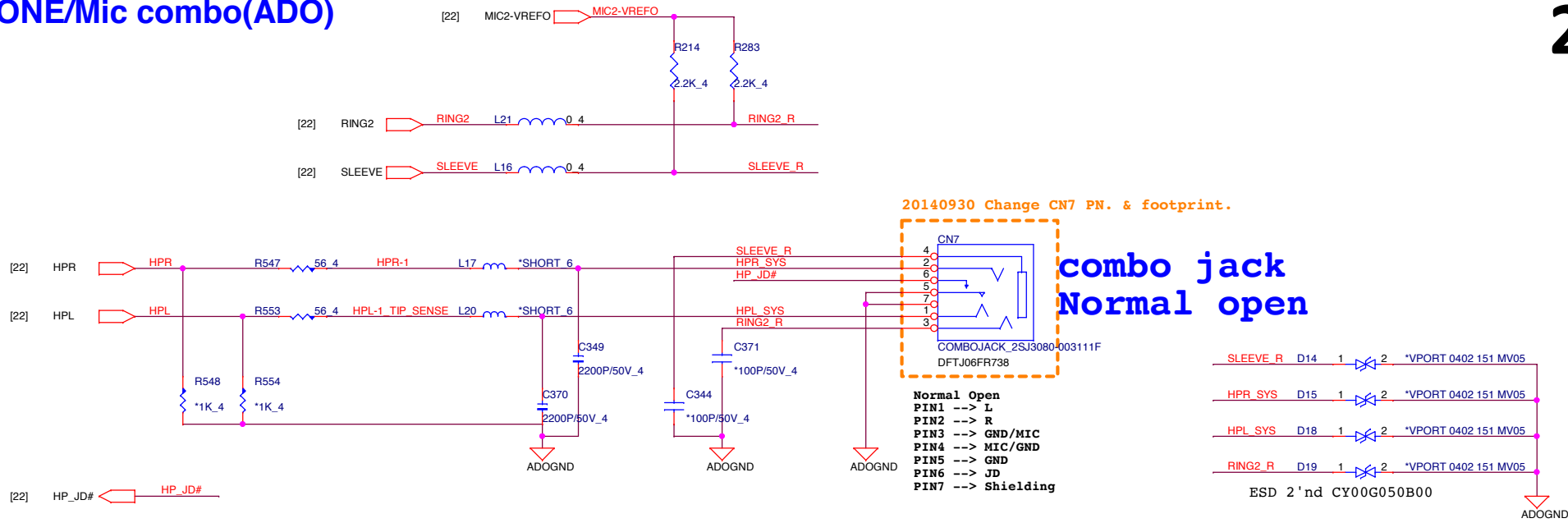
20140922 Remove A-MIC, add D-MIC same as Hugo(ZHQ)

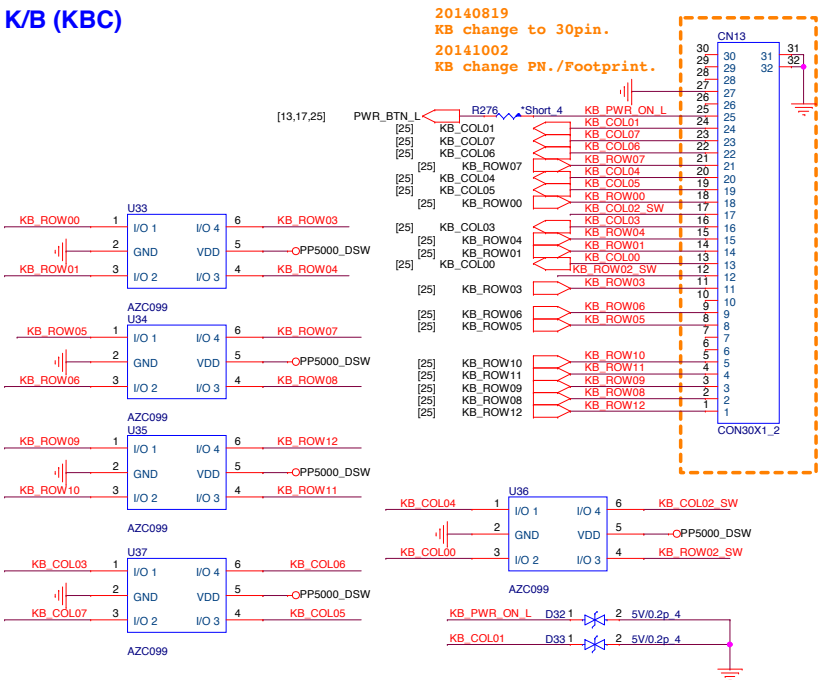


footprint 88266-040xx-xxx-4p-1

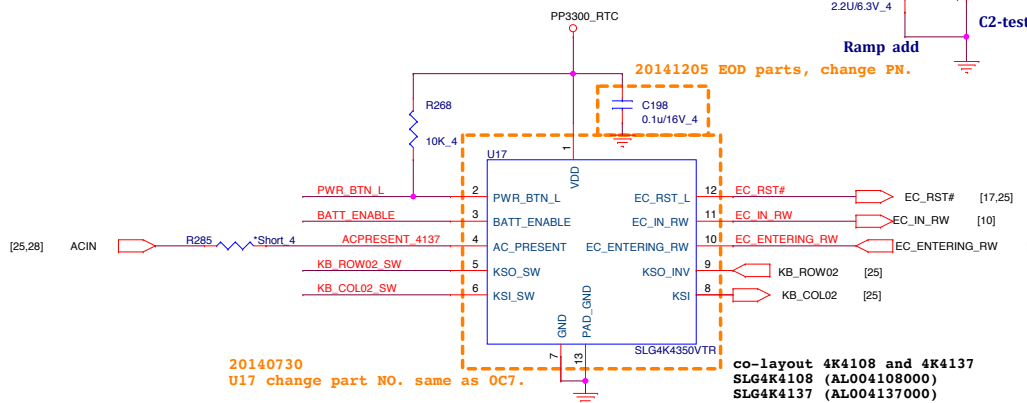
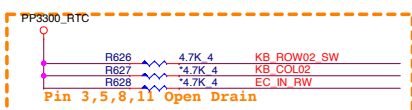


HEADPHONE/Mic combo(ADO)



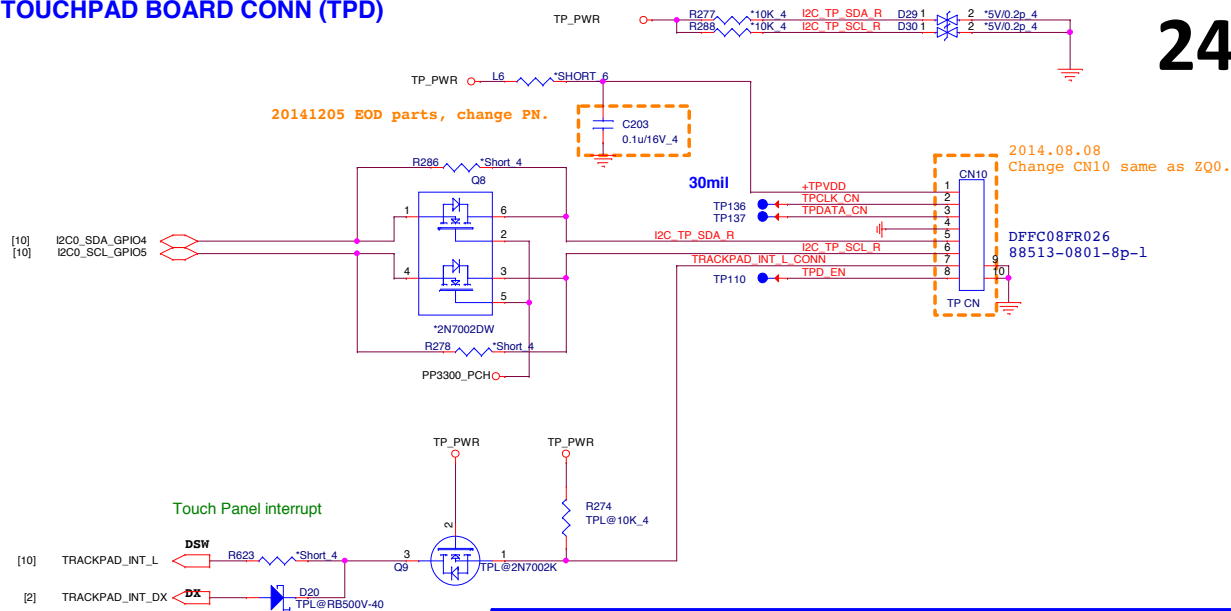


HOLELESS RESET 2-CHIP(KBC)

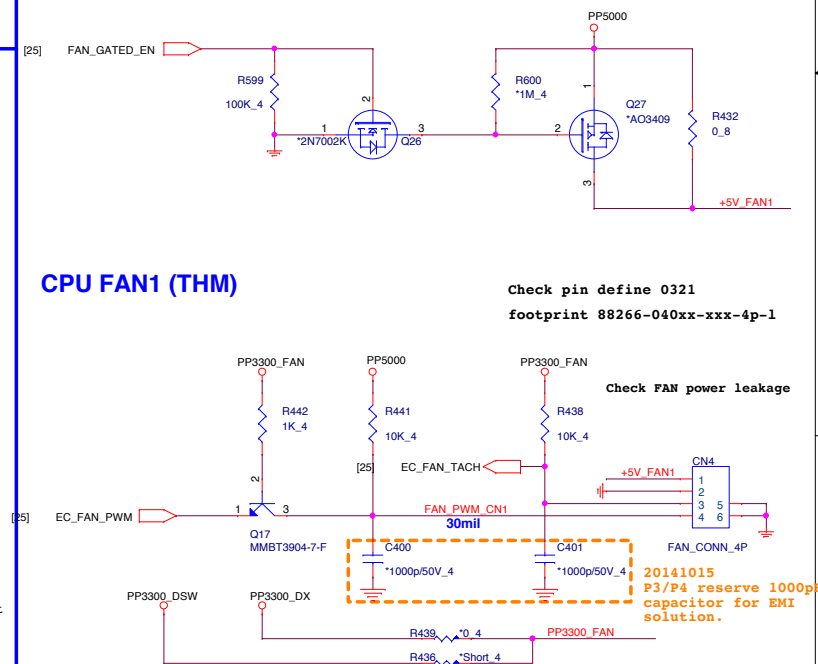


co-layout 4K4108 and 4K4137
SLG4K4108 (AL004108000)
SLG4K4137 (AL004137000)
4K4137 PIN3 is BATT_ENABLE
4K4137 PIN4 is AC_PRESENT

TOUCHPAD BOARD CONN (TPD)



CPU FAN1 (THM)



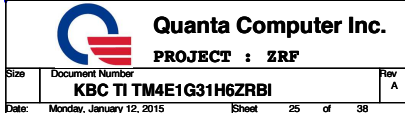
```

Check pin define 0321
footprint 88266-040xx-xxx-4p-1

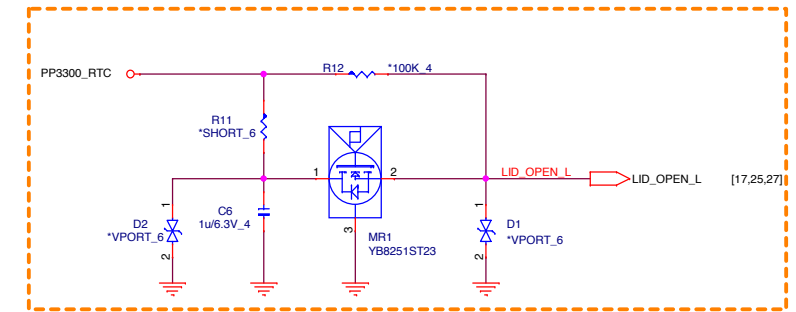
```

Check FAN power leakage

20141015
P3/P4 reserve 1000pF
capacitor for EMI
solution.

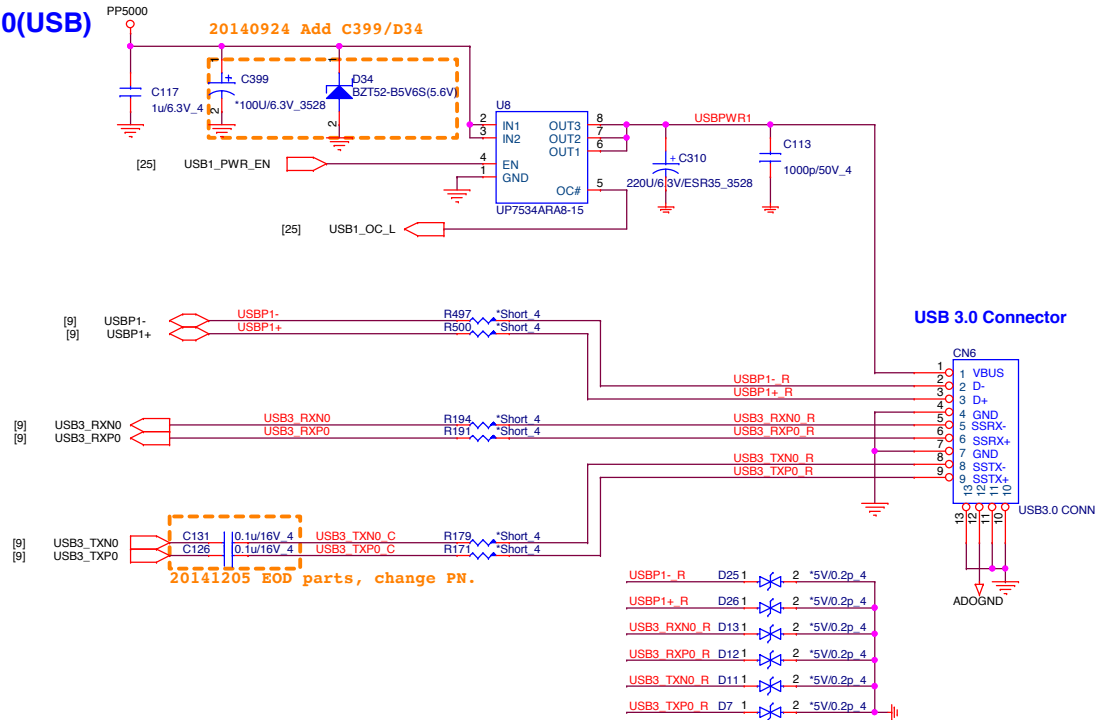


Lid Switch (HSR)

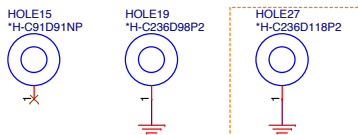
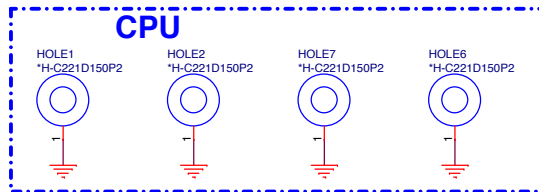
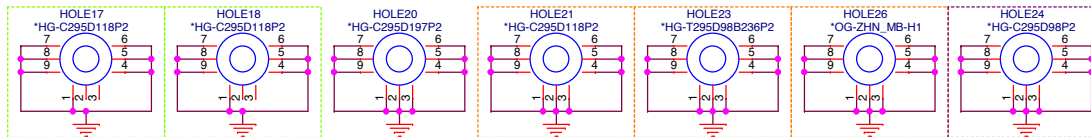


20140923 Add Lid Switch (HSR)

USB3.0(USB)



HOLE(OTH)



20140828

1. Add HOLE27
2. Change HOLE17/HOLE18/HOLE21/HOLE22 /HOLE23/HOLE26 footprint
3. Remove HOLE9/HOLE16

20140829

1. Change HOLE27 footprint
2. HOLE17/HOLE18/HOLE22 remove Pin1/Pin2/Pin3

20140901

1. Remove HOLE22

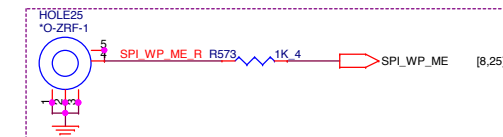
20140923

1. Remove battery enable, change to HOLE24

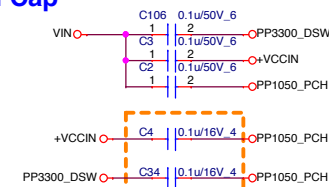
20140926

1. HOLE24 change footprint.
2. HOLE25 Add more 2pin & change footprint.
3. Remove HOLE3/4/5/8/10/11/12/13/14.

ROM WP#

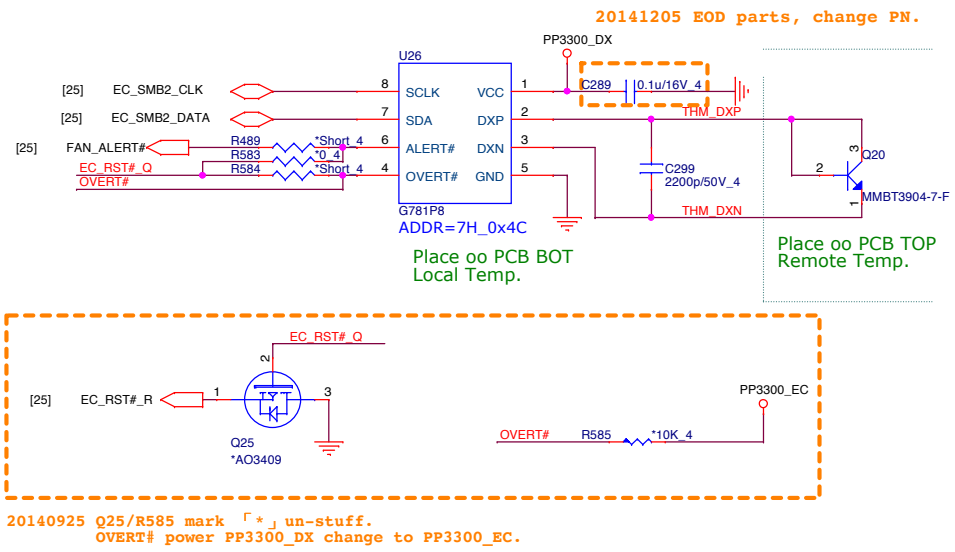


EMI Cap

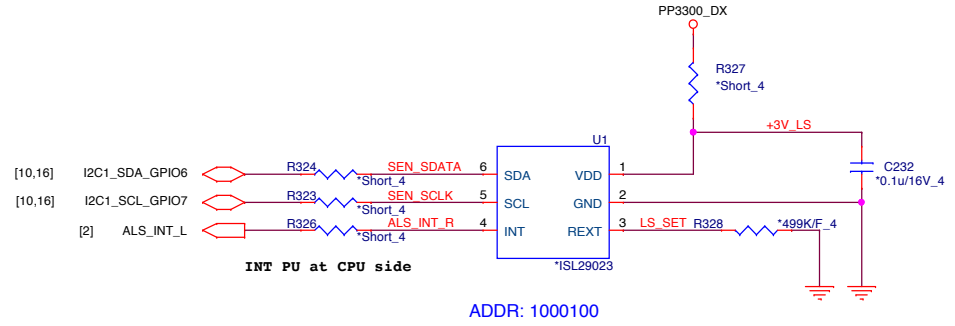


20141205 EOD parts, change PN.

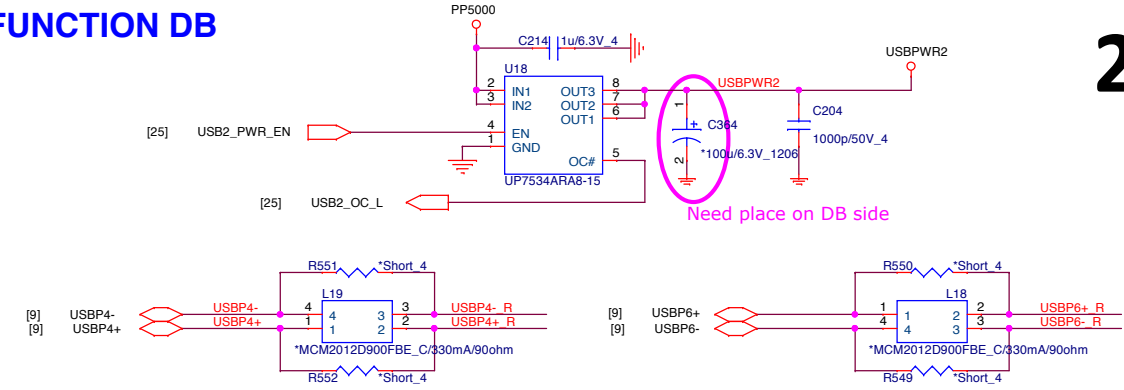
Thermal Sensor(THM)



Light sensor & TP (ALS)

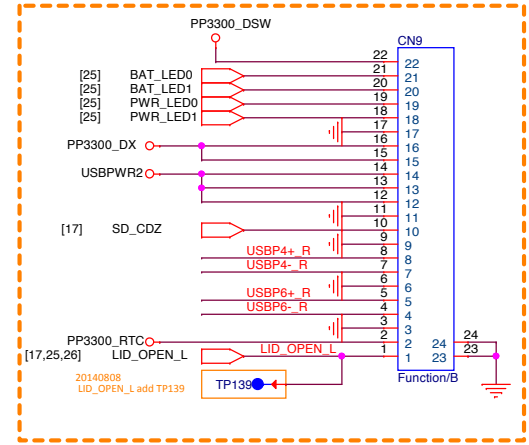


FUNCTION DB




HSR	+3VPCU
	LID_OPEN_L
	GND
LED	+3VPCU
	LED x 4
	GND
USB	+3V x 2
	GND x 2
	USBP0+
	USBP0-
CR	CR_DET
	+3V x 2
	USBP6+
	USBP6-
	GND x 2
LID	PP3300_RTC
	LID_OPEN_L

footprint 50501-0220n-v01-22p-1
DFFC22FR019

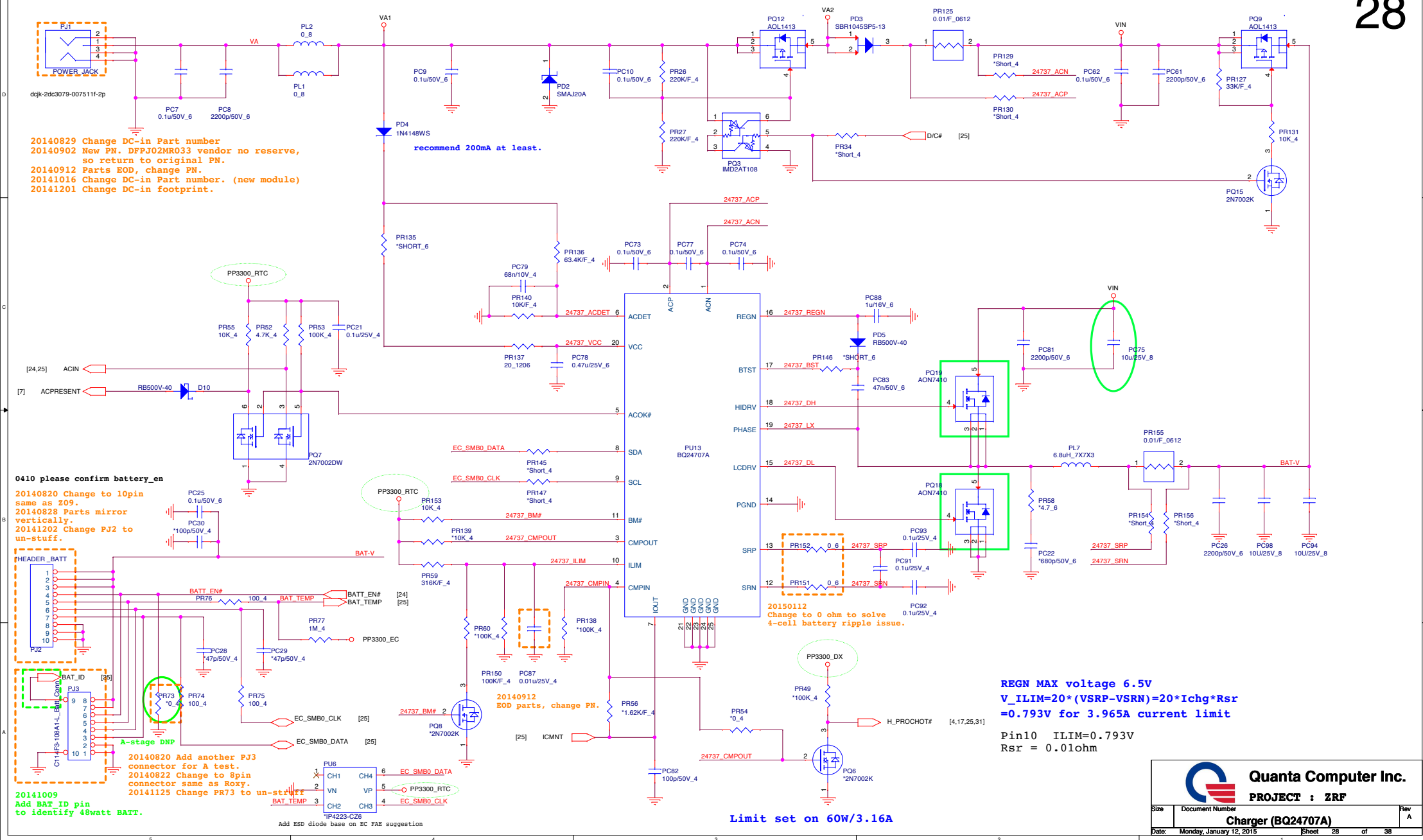


20140728 Modify to 22pin.
20140819 Change footprint



Quanta Computer Inc.
PROJECT : ZRF

Size	Document Number	Rev
	DB/ALS/Thermal sensor	A
Date:	Monday, January 12, 2015	Sheet 27 of 38



TDC : 0.75A
PEAK : 1A
Width : 40mil

TDC : 0.38A
PEAK : 0.5A
Width : 20mil

+DDR_VTT_RUN

Greater than or equal 40mil

1.35 Volt +/- 5%
TDC : 3.35A
PEAK : 4.46A
OCP : 6A
Width : 140mil

20141205 EOD parts, change PN.

VREF=1.8V

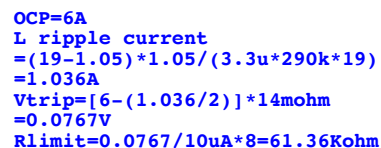
PCH_SLP_S3_L PR163 *Short_4 51216_S3
PCH_SLP_S5_L PR80 *0_4

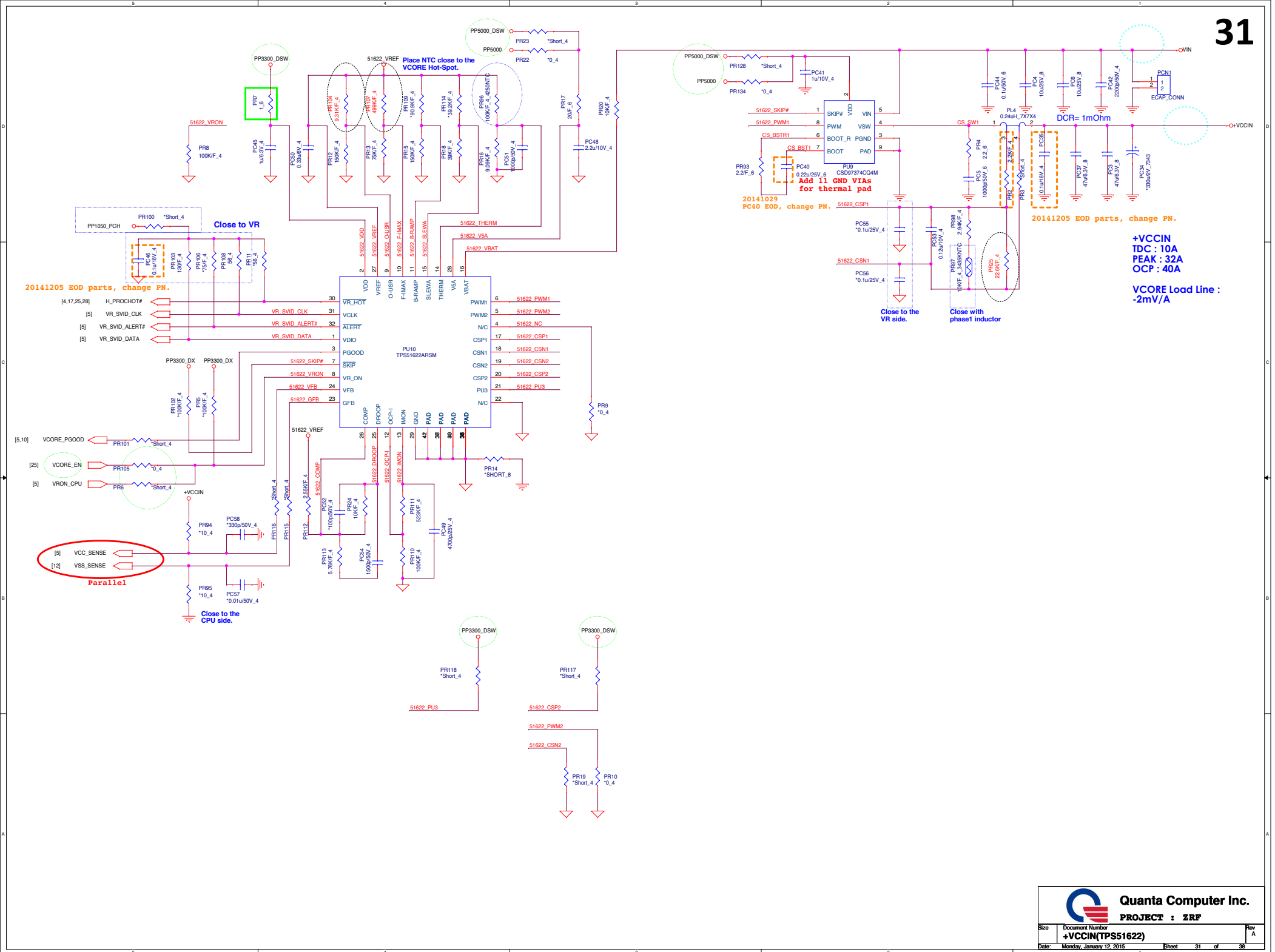
OCP=6A
L ripple current
= $(19-1.35) \times 1.35 / (3.3\mu \times 400k \times 19)$
=0.95A
Vtrip=[$6-(0.95/2)$]*14mohm
=0.07735V
Rlimit= $0.07335 / 10\mu A \times 8 = 61.88Kohm$

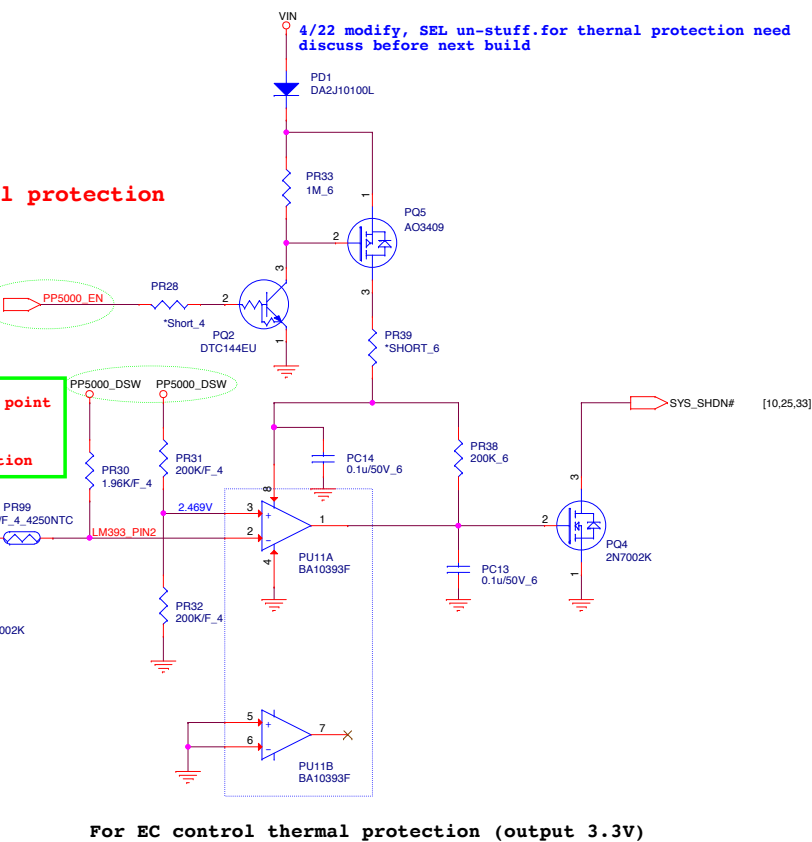
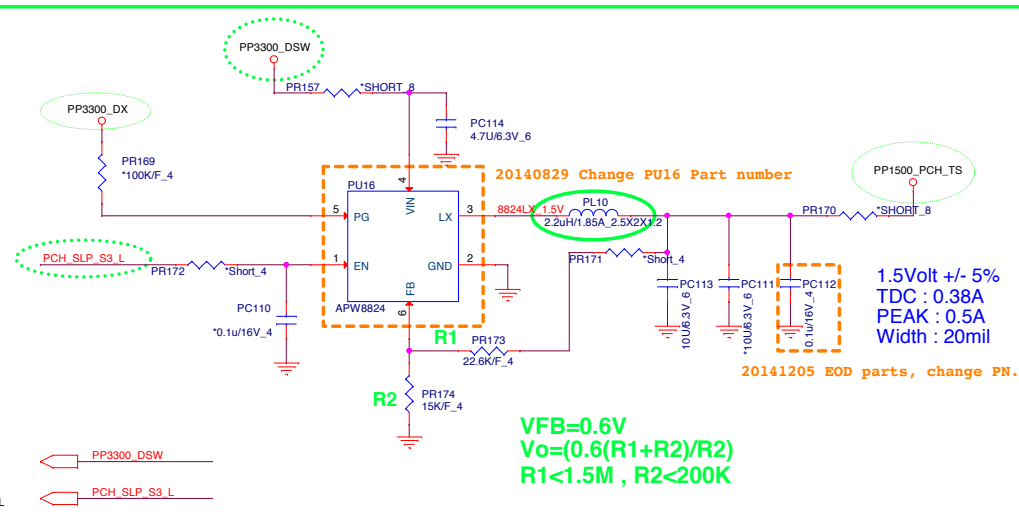
20140912
EOD parts, change PN.

Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (main on off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF



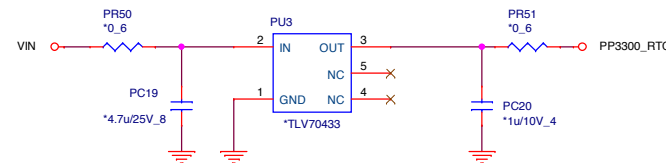
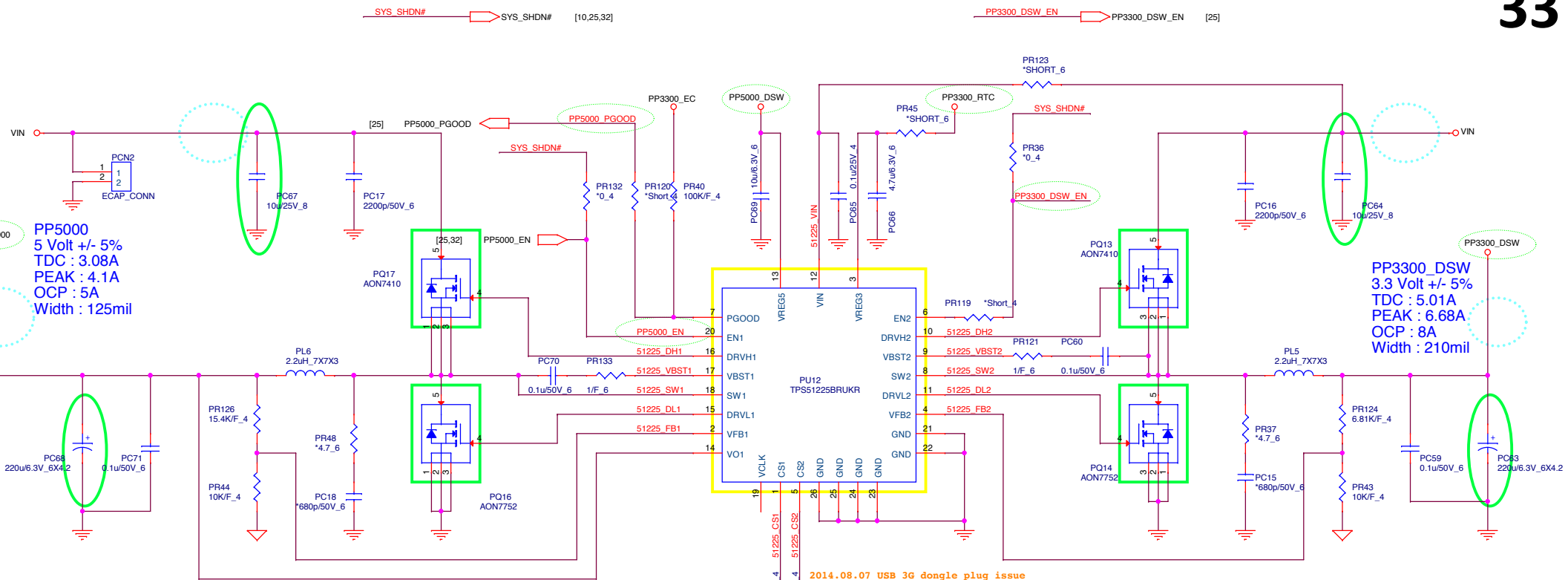






Quanta Computer Inc.


PROJECT : ZRF

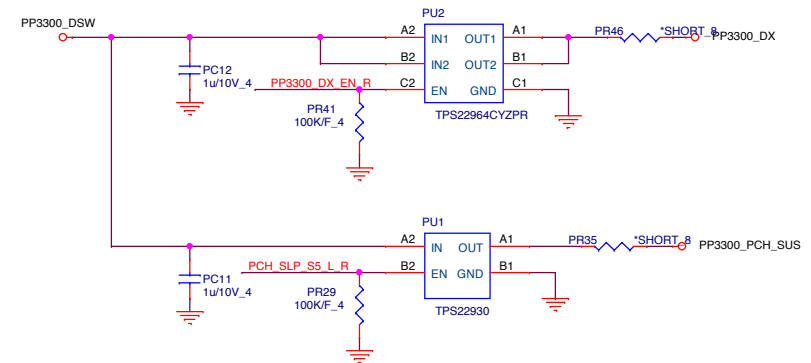
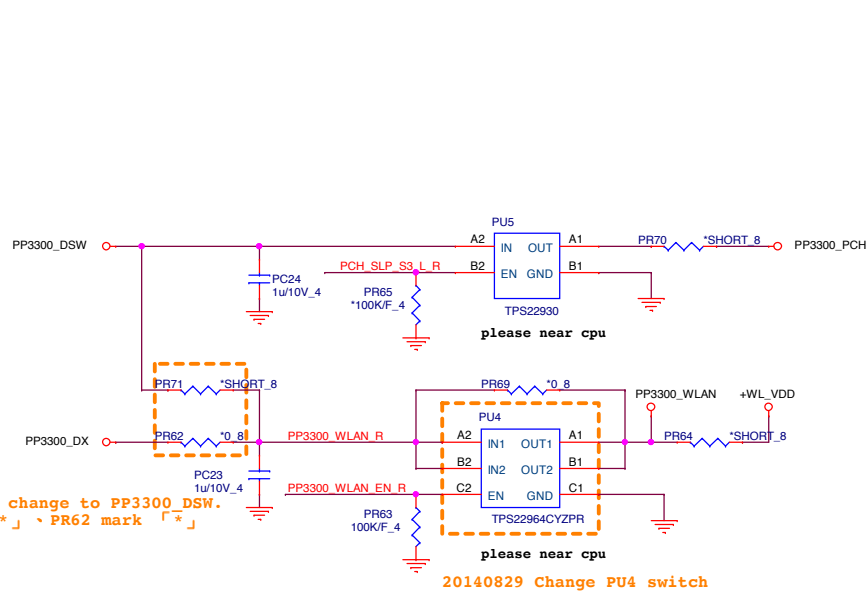
Size	Document Number	Rev
	+1.5V/Thermal protect	A
Date:	Monday, January 12, 2015	Sheet 32 of 38





[7,13,25,29,30,32] PCH_SLP_S3_L  PCH_SLP_S3_L PR166 *Short_4 PCH_SLP_S3_L_R

[25] PP3300_DX_EN  PP3300_DX_EN PR167 *Short_4 PP3300_DX_EN_R

[10,19,25] PP3300_WLAN_EN  PP3300_WLAN_EN PR168 *Short_4 PP3300_WLAN_EN_R



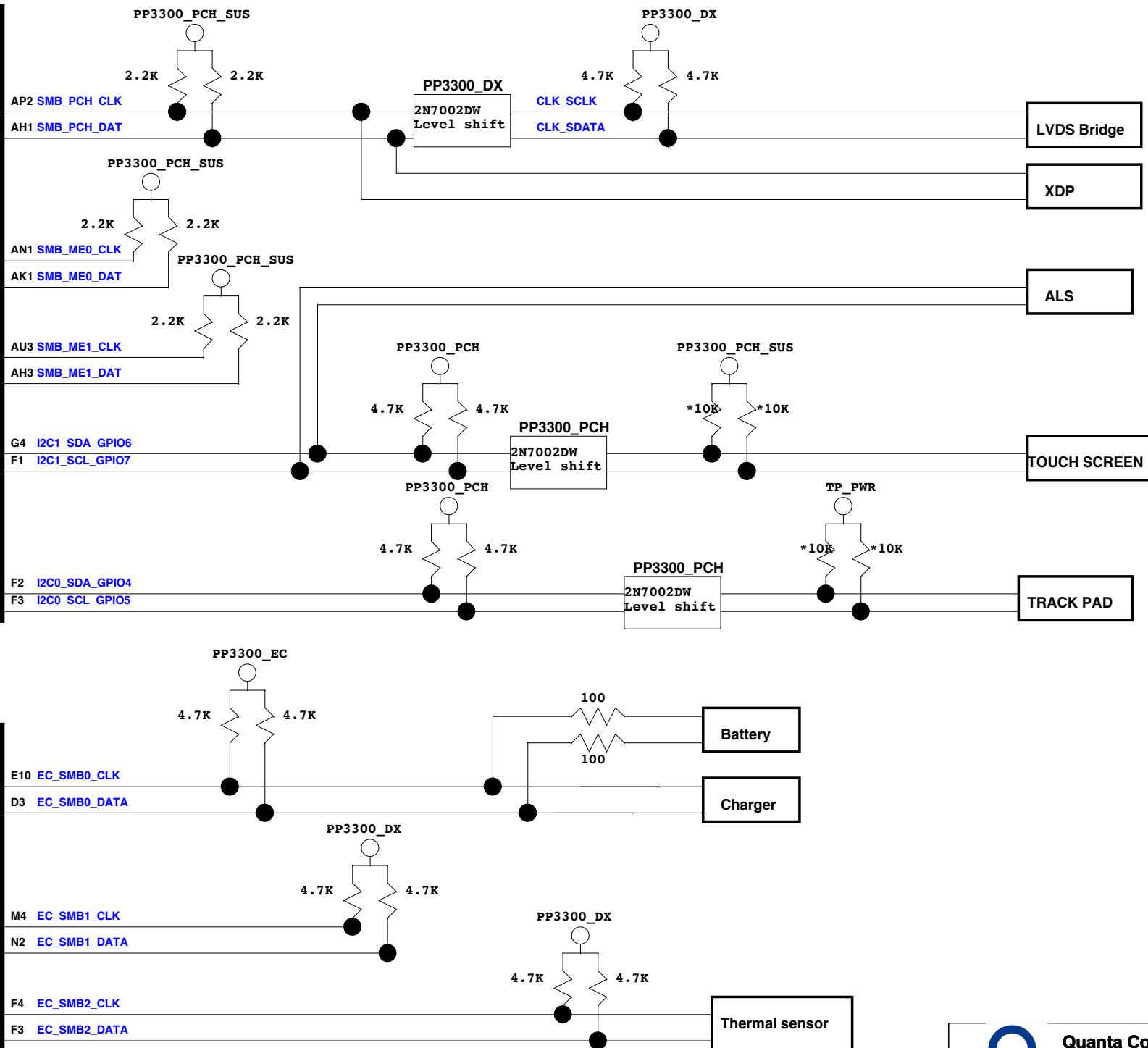
[7,25] PCH_SLP_SUS_L  R115 *Short_4 PCH_SLP_S5_L_R

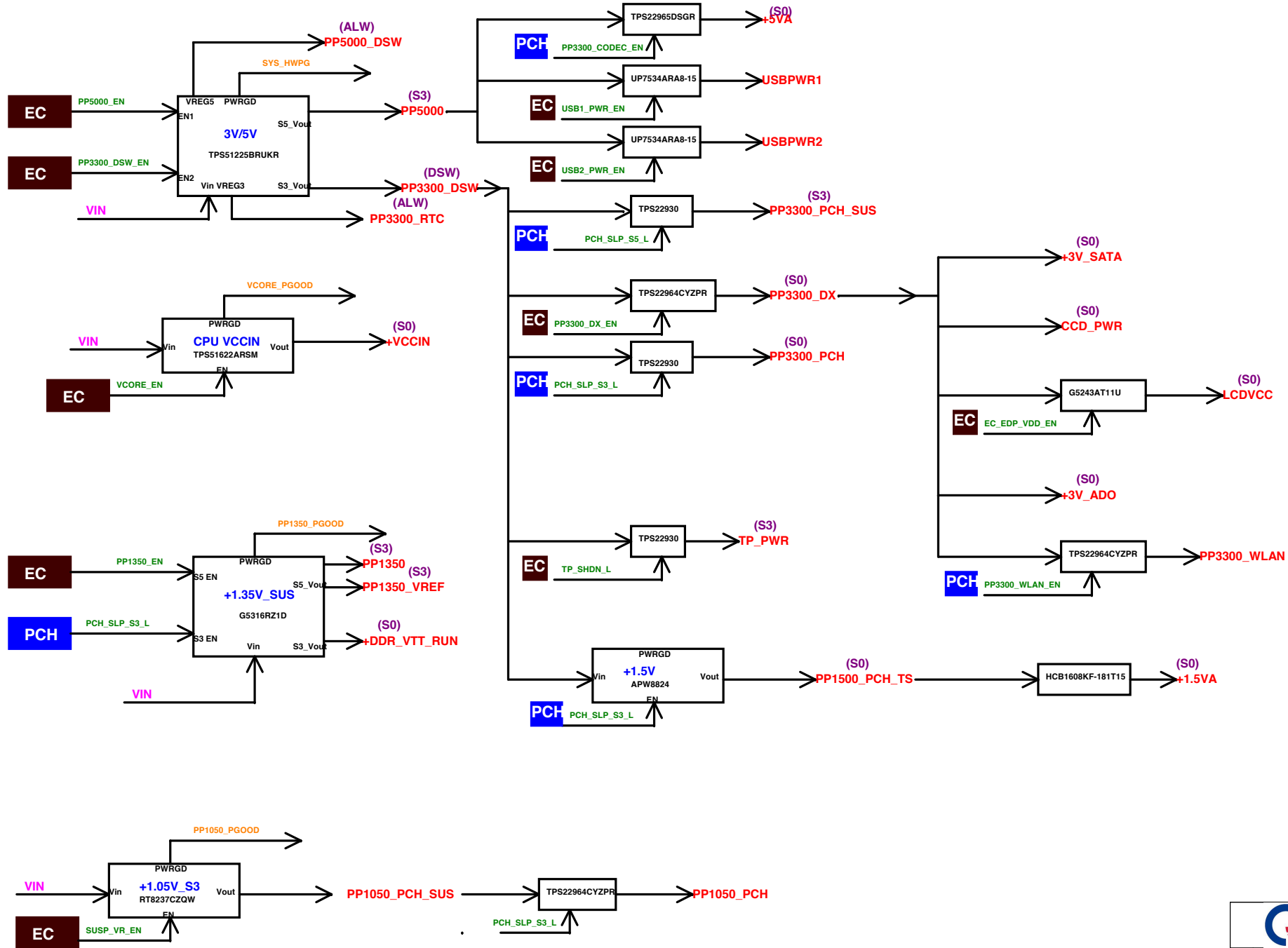
[7,13,25,29] PCH_SLP_S5_L  PCH_SLP_S5_L R112 *0.4

**Haswell
ULT**

I2C

KBC
TI
SMBUS





Model	Version	CHANGE LIST		
ZRF	1A-1	20140728: Add source change to LED board, (HBI) 20140728: Page24: Change touchpad cone, as Hago, (CN10) (change to larger pitch) 20140728: Page27: Ledmatrix cone, 20 pin change to 22 pin, (CN9) 20140728: Page26: Add on Track Pad Input for linkage issue		
	1A-2	20140730: Page24: I/F change part NO, same as B-C7.		
	1A-3	20140804: Page16: LCD cone, 30pin change to 40pin, 1 LED change to 2 LED, (CN3)		
	1A-4	20140806: Page16: touchpad level shift remove Q13 change to U8. 20140807: Page26: Remove R508A, Q10 MOS (channel change to 3 channel, remove USBP4+ + USBP4+ pins, remove NGFF PCH, pins remove NGFF CLK pin, GPIO9 pull high, System S733 change part NO, (P12)		
	1A-6	20140808: Page16: Touch panel INVERTED pins mark ϵ^+ ϵ^- 20140808: Page24: Change CN3 cone as ZDF. 20140808: Page27: LED GREEN 5-pin add TP129		
1A-7	20140811: Page19: 1. I/F, DISASSEMBLE 3, 1 GPIO19 pull high to PP300_PCH_SIS 20140811: Page27: Remove light sensor.			
1A-8	20140812: Page16: touchpad level shift remove U8 change to F1T1M8. 20140812: Page22: Color pin27 and 100K resistance			
1A-9	20140819: Page24: KR change to 30pin, 20140819: Page27: CR cable connector change footprint			
1A-10	20140828: Page19: Wi-Fi on board IC change to same as Z80 connector, 20140828: Page20: P33 battery connector change to 50pin same as Z80, 20140828: Page26: Add another P33 battery connector for A test.			
1A-11	20140821: Page16: LCD cone, ECU, SDA, GPIO6, CONN pins reserve a 10pin capacitor.			
1A-12	20140822: Page19: Wi-Fi return to another onboard module 7268SDW 20140822: Page20: P33 battery connector change to 50pin same as Roxy.			
1A-13	20140825: Page25: Change power capacitor value.			
1A-14	20140826: Page28: Change power output MOS/capacitor, (PQ18 + PQ19 + PCT5) 20140826: Page29: Change power output MOS/capacitor, (PQ20 + PQ21 + PCT3) 20140826: Page28: Change power output MOS/capacitor, (PQ19 + PQ11 + PCT7) 20140826: Page32: Change I/F solution IC, 20140826: Page29: Change power MOS/capacitor, (PQ13 + PQ14 + PQ16 + PQ17 + PC63 + PC34 + PC37 + PC60) 20140826: Page19: Wi-Fi PCB TX/RX wrap, and RX add capacitor, 20140826: Page27: Change Wi-Fi onboard module 7268SDW footprint.			
1A-15	20140827: Page19: Pin W, DISASSEMBLE 10, 2014081222 add 100K resistance pull-down. 20140827: Page16: LCD cone, change PN / footprint same as ZQ0, 20140827: Page18: Change HDMI cone / footprint			
1A-16	20140828: Page20: BATT cone, P12 remove vertically, 20140828: Page26: 1. Add H0K E27, 2. Change H0K E12 to H0K E21 H0K E22 H0K E23 H0K E26 footprint, 3. Remove H0K E12 H0K E16, 20140828: Page19: Wi-Fi 100K resistance B01 B0A2 mark ϵ^+ ϵ^-			
1A-17	20140828: Page20: Change LEO P14 coil-back 20140828: Page28: Change P31 DC-EN part number, 20140828: Page26: Change I/F P14 part number.			
1A-18	2014092: Page26: DC-in return to original PN.			
1A-19	20140909: Page19: Change Wi-Fi onboard module 7268SDW footprint.			
1A-20	20140912: Page16: C16 EOD, change PN, 20140912: Page28: C776, 20K 3015 EOD, change PN, 20140912: Page22: L4/L7 EOD, change PN, 20140912: Page28: C2001, 302K 3015 EOD, change PN, 20140912: Page28: PC-WIFI EOD, change PN, 20140912: Page29: PC-100 EOD, change PN, 20140912: Page30: P803 EOD, change PN.			
1B-1	20140922: Page22: A-MBC change to D-MBC (same as Hago/Z80).			
1B-2	20140923: Page26: Add L4 Switch (H88) 20140923: Page22: A-MBC, PWB remove PWB_PCH, change use PP300_PCH, 20140924: Page26: USB3.0 USB P1972 add C399D3A.			
1B-4	20140925: Page27: Thermal MOSFET Q25/Resistance R55 mark ϵ^+ -no-stuff, OVERHEAT pin/P5200_DS change to PP300_EC.			
1B-5	20140926: Page22: Change CN3 footprint.			
1B-6	20140930: Page23: Change CN7 Audio Jack PN, & footprint, 20140930: Page16: Change CN3 LCD cone, footprint, 20140930: Page25: Change US EC, PN.			
1B-7	20141002: Page24: KR change PN, footprint.			
1C-1	20141009: Page25: EC N12 pin add BATT_ID to identify different BATT, cone, & add B633 pull high. 20141009: Page20: BATT, cone, and BATT_ID to identify different BATT.			
1C-2	20141014: Page19: Change Wi-Fi onboard module 7268SDW PN.			
1C-3	20141014: Page24: Fan connector Pin3/Fan reserve 100nF capacitor for EMI solution.			
1C-4	20141016: Page26: Change DC-in PN, (new module)			
1C-5	20141028: Page34: LEO P14 power change to PP300_DS/W, P871 cancel ϵ^+ + P862 mark ϵ^+ ϵ^-			
1C-6	20140921: Page16: LCD cone, footprint return to ZQ0, 20141021: Page13: Add register module TTP C18 P1971 add PP180_PCH_SIS, P10 PP180_PGOOD change to VCYST_PWDZD, 20141029: Page31: PC40 EOD, change PN.			
1D-1	20141029: Page31: PC40 EOD, change PN.			
1D-2	20141112: Page32: C193 change to 0.1uF, 20141112: Page16: add 0 ohm resistors change to short pad.			
1D-3	20141108: Page22: Page25: change 102302 PN.			
1D-4	20141128: Page28: Change EC, BRD, ID, ID2 change to High, ID3 change to Low, because EC change code.			
1D-5	20141112: Page28: Change P873 to no-stuff.			
1D-6	20141201: Page21: Change TP41 power, 20141201: Page21: DMC2, CLK, L, reserve 22pF capacitor, 20141201: Page28: Change EC new PN, 20141201: Page27: Shift L12, remove R731/R732, 20141201: Page28: Change DC-in footprint.			
1D-6	20141202: Page28: Change P22 to no-stuff.			
1D-7	20141205: CH402K, D803 EOD parts, change PN, CH408K, B08B, 20141205: CH408K, B03 EOD parts, change PN, CH408K, B08B, 20141205: C2521, 218 0.1 EOD parts, change PN, C2522, 202 B08B, 20141205: R404, R508, R509, R510, R511, R512, R513, R514, R515, R516, R517, R518, R519, R520, R521, R522, R523, R524, R525, R526, R527, R528, R529, R530, R531, R532, R533, R534, R535, R536, R537, R538, R539, R540, R541, R542, R543, R544, R545, R546, R547, R548, R549, R550, R551, R552, R553, R554, R555, R556, R557, R558, R559, R560, R561, R562, R563, R564, R565, R566, R567, R568, R569, R570, R571, R572, R573, R574, R575, R576, R577, R578, R579, R580,			
1D-8	20150109: Page28: Change I/F EC IC, PN, for MP.			
1D-9	20150112: Page28: Change resistance PR151/PR152 to 0 ohm to solve 4-ohm ripple ripple issue.			
DOC NO.	PROJECT MODEL: Part Number: Change	APPROVED BY: DRAWING BY: Change	DATE: REVISION: Change	Quanta Computer Inc. PARENT EMP Change